INVESTIGATION OF MULTILAYER PRINTED CIRCUIT BOARD MATERIALS

FINAL REPORT

Prepared under Contract No. NAS 8-21477

by

North American Rockwell Corporation

MARSHALL SPACE FLIGHT CENTER

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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By J. E. Meinhard

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INVESTIGATION OF MULTILAYER PRINTED CIRCUIT BOARD MATERIALS

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SUMMARY

Inherent in conventional multilayer board manufacturing methods are a number of materials factors critical to product reliability. One of the more important problems relates to through-hole interconnections which, in present practice, involves the use of two highly mismatched materials: copper and glass-epoxy laminations. The divergence of these materials in thermal expansion properties alone, particularly in the z-direction (normal to circuit planes and parallel to interconnections), constitutes a hazard to circuit continuity in any environment where cyclic or repetitious temperature excursions are imposed on the board. Such environmental stresses cannot be prevented without prohibitive expense, and the board therefore becomes a jeopardy to the mission it is supposed to serve. This risk of in-time electrical failure is augmented not only by other materials interactions but also by certain techniques presently required in board fabrication.

The purpose of this program is to reduce the present process liabilities by developing a three-dimensional circuit technology which employs materials and techniques of improved compatibility.

To achieve this result a multilayer board technology utilizing a polyimide plastic as the dielectric and a pyrolyzed polyacrylonitrile as a portion of the conductor network has been developed and tested. The polymide, in addition to providing a closer thermal expansion match, even with metallic conductors, proved adaptable to fabrication techniques and superior in stability to physical stresses of all types. The pyrolyzed polyacrylonitrile was selected as the major component of an organic z-direction conductor after screening several classes of promising organic conductive solids. Thin film metallized circuits were employed in the x, y-planes.

A set of internally compatible procedures and sequences was developed for the fabrication of electrically functional boards capable of reliable connection to external circuitry. A total of 11 boards were completed, each containing four levels of internal circuitry and one exposed top circuit. Five of the boards were subjected to 427 environmental stress cycles over the temperature range, -55 to +100 deg C, the final 211 cycles being conducted at 90 percent relative humidity. Electrical tests before, during and after the cycling disclosed that this treatment was survived by approximately 75 percent of the circuits and that it had virtually no adverse effect on dielectric performance.

The only solder connections to the boards lost during cycling were those known to be initially defective. The utilization of a thermal cycling treatment as a procedure for eliminating potential failures was suggested by the electrical data. A statistical evaluation of these data pointed to a high degree of materials compatibility with respect to thermal expansion properties but a lower degree of compatibility in regard to the combined effects of water absorption and the thermal cycling.

INTRODUCTION

During the first year of this program it was shown that a process utilizing highly cured polyimide as the isolation dielectric, and other organic substances for at lease a part of the conductor system, was technically feasible. The present report briefly reviews these results and describes subsequent effort in which substantial steps have been taken to reduce to practice the concepts previously developed.

The epoxy-glass laminate system is prone to certain types of failure that can be traced to incompatibilities inherent in the materials used. Outstanding among these is the highly anisotropic thermal expansion of the laminate system which ideally should accommodate simultaneously to thermally induced dimensional changes in copper conductors in the x-, y- and z-directions of the board. The development of a polyimide dielectric system applied layer-by-layer, yet molecularly interlocked to produce the effect of an isotropic medium, offered a promising route around the laminate problem. In particular, the large expansion mismatch in the z-direction characteristic of the laminates could be avoided.

To advance even further the over-all compatibility of the materials employed, replacement of metallic conductors with organic conductors (or at least partially organic conductors) also was investigated. A survey of various materials to fill this role resulted in the following candidates: pyrolyzed polyacrylonitrile, sulfur derivatives of polynuclear aromatics (such as dibenzanthrone) and charge transfer complexes of tetracyanoquinodimethan with vinylpyridine polymers.

The techniques of utilizing such materials, since these required an approach entirely different from laminate technology, also had to be worked out. The polyimide layers, for example, not only had to be molecularly bonded to each other but also required a means of via etching in the z-direction (i.e., the direction normal to the plane of the board) in order to provide paths for conductors connecting one layer of circuitry with another or with external electrical conductors. This was achieved by taking advantage of the solubility of undercured polyimide in basic solutions. Etching of vias with ammonia solutions through a suitable mask was found to be feasible, after which the mask could be removed and the polyimide cured to a highly insoluble condition.

Except for some rudimentary experiments, techniques for filling the vias with z-direction conductor were largely unexplored. This was due to the fact that an application technique would be highly dependent on the organic material employed, a choice that had not yet been made at the end of the first year of the program. It was shown, however, that polyacrylonitrile, applied as a thin, coherent film from solution, could be pyrolyzed to a black coating under the same thermal conditions as a normal polyimide cure cycle. If sufficiently conductive, these pyrolyzed films could become a convenient means of filling the vias.

Various other process details had to be worked out, such as the deposition and delineation of metallized circuitry on polyimide surfaces, the application and removal of photopolymers, and of mask materials, for definition of vias as well as circuits and the special composition required by the top circuit layer to permit solder connections to be made to it. These objectives were achieved and, at least to a limited extent, the application of these process steps in sequence was shown to be feasible.

It remained to prove out this apparent feasibility in terms of producing functioning boards and of demonstrating the functional survival of these boards under environmental stress which would act as an indicator of the inherent compatibility of the materials used. In achieving these objectives it was proposed that a minimum of four boards be fabricated, two on aluminum substrates and two on polyimide (Vespel) substrates. In each pair, one board was to have organic-filled z-direction conductors the other, gold-filled z-direction conductors. Inclusion of metal-filled conductors was proposed not only for comparative purposes, but because of the incomplete stage of development of the organic conductors. The boards were to have multiple circuit layers plus a top layer in which all vias terminated and to which external components could be soldered. Electrical performance of the boards was to be monitored before, during and after an environmental stress regime minimally including thermal cycling and exposure to humidity. Following an evaluation of the test results the boards were to be delivered, along with their test histories, to the National Aeronautics and Space Administration for further examination. Achievement of these objectives is the subject of this Final Report.

ARTWORK USED IN BOARD FABRICATION

In reducing to practice the multilayer board technology evolved in the preceding phase of this program, it was necessary first to reach a decision on the artwork to be used in board fabrication. To accomplish this it was necessary to establish certain criteria to act as a guide to selection (if possible), or design, of the artwork. These criteria required that the artwork be capable of demonstrating, in a finished board, minimally the following:

1. Z-direction circuit continuity, 1 to n layers.
2. X, Y conductivity, function of line width and other dimensional and material parameters.
3. X, Y dielectric isolation proximity limits.
4. Z-direction dielectric integrity.

After reviewing a number of sets of artwork, selection was made which provided z-direction vias in four diameters ranging from 0.040 to 0.075 inches, x, y line widths ranging from 0.005 to 0.040 inches, x, y dielectric isolation limits down to 0.005 inches and a thoroughly adequate test pattern for z-direction dielectric integrity. This artwork, which was designed originally for use with conventional laminate technology, included a top and a bottom circuit layer and six internal circuit layers. It was decided, however, that a five-layer board, consisting of four internal layers and one top layer, would serve adequately in the demonstration of program objectives. The patterns utilized are reproduced (1:1) in Figures 1 through 6.

Upon acceptance of a set of artwork the substrate dimensions were fixed (at 4-3/4 by 5-3/4 in.) and orders for substrate fabrication placed. The requirement of substrates as a foundation for the build-up of circuit layers is one consequence of the departure from conventional laminate technology. Board substrates were cut from both polished aluminum and Vespel (du Pont TM), a fully cured polyimide sheet available in the dimensions, 12 x 12 x 0.25 in. The Vespel proved to be machinable and was cut into substrates 1/16 to 3/32 in. thick. The surfaces were milled to reduce surface roughness.

In initial experiments a first dielectric layer of polyimide was applied to several aluminum substrates using a spinning process normally employed in photoresist application. To do this it was necessary to make equipment modifications to accommodate the larger substrate dimensions. The films so formed were thermally cured up to 315 deg C. Thickness was estimated to be uniform at 0.0002 to 0.0005 in. with very few visible flaws.

A chrome (200 Å)-gold (8000 Å) layer was vacuum deposited on the dielectric layer followed by application of Riston (du Pont TM) and photoetching through mask "T" of the artwork (Figure 6). Visual inspection revealed no flaws in the conductor patterns. Electrical tests revealed dielectric isolation in excess of 10^5 ohms at the closest conductor spacings (5 mils) and a complete absence of z-direction pinholes. These results were taken as a reconfirmation of the inherent adequacy of the process concept.

Z-DIRECTION CONDUCTOR

Metal-Filled Composite

Gold powder of 0.2 micron particle size was procured* for preparation of z-direction conductors. The gold powder was mised with polyimide varnish (du Pont

*From Engelhard Industries

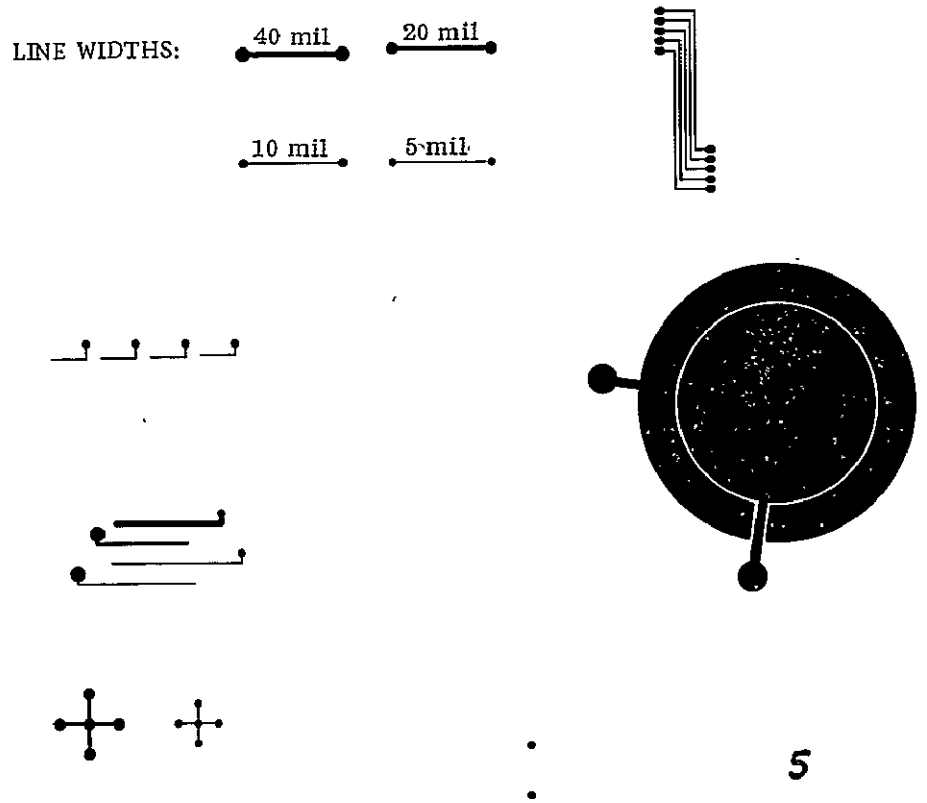


Figure 1. Circuit Pattern 5 of Artwork

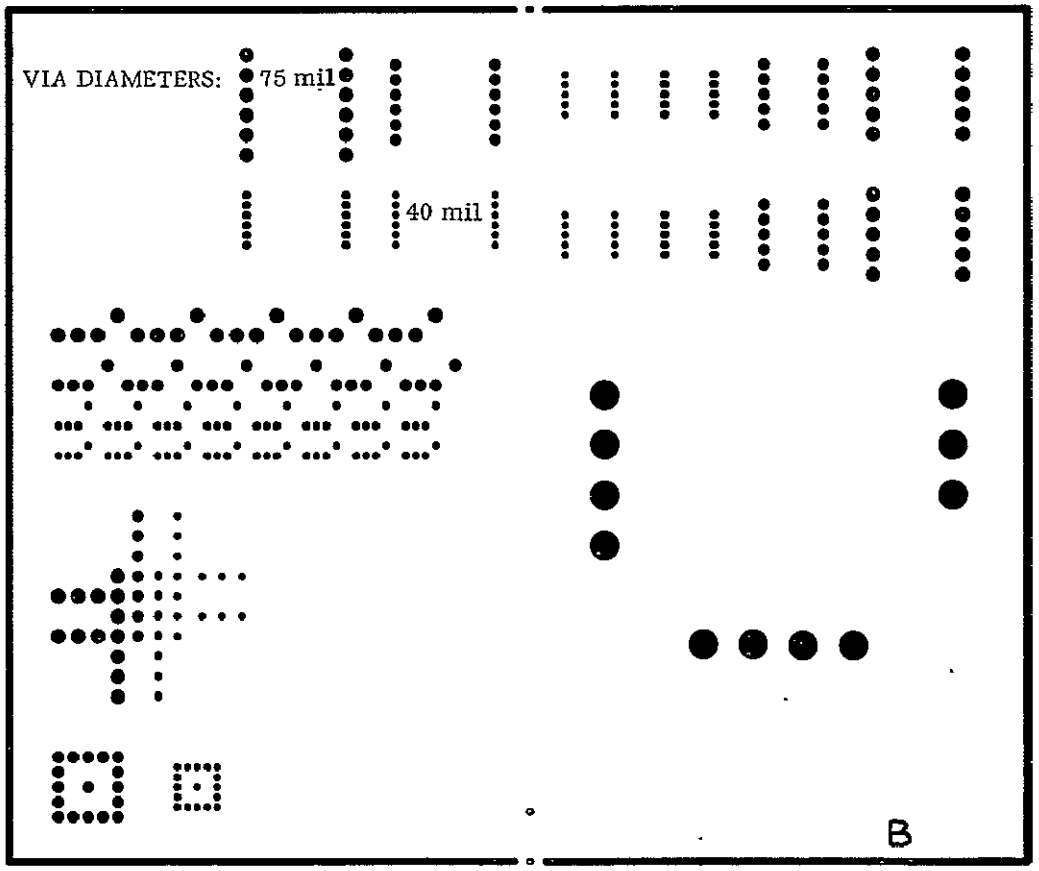


Figure 2. Via Pattern "B" of Artwork

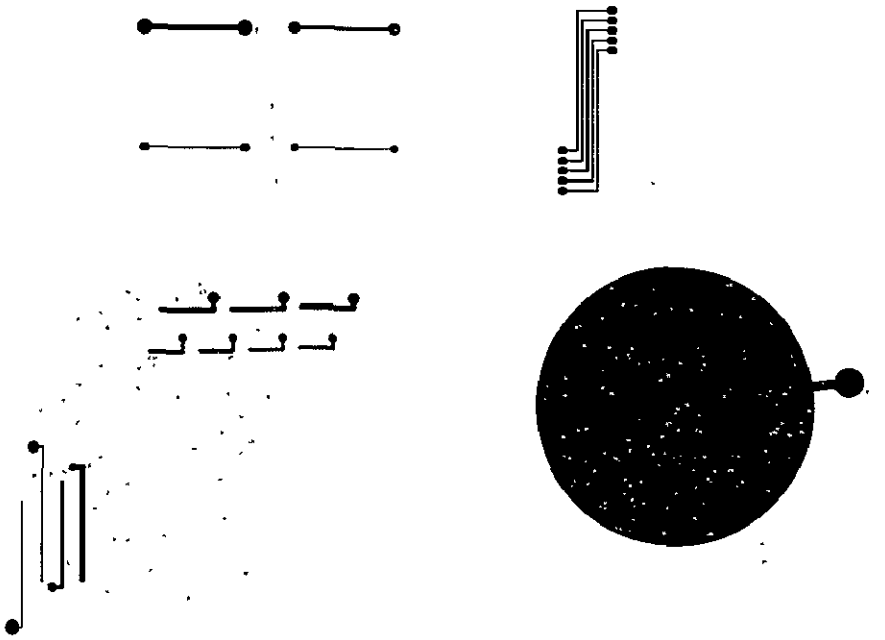


Figure 3. Circuit Pattern 4 of Artwork

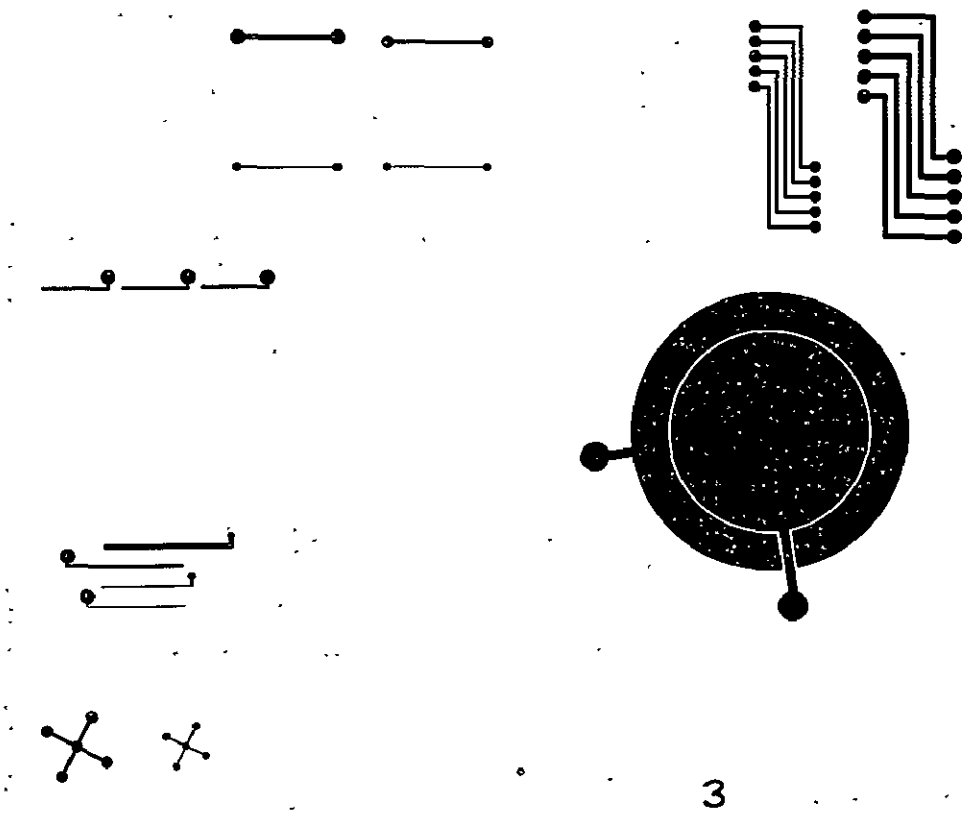


Figure 4. Circuit Pattern 3 of Artwork

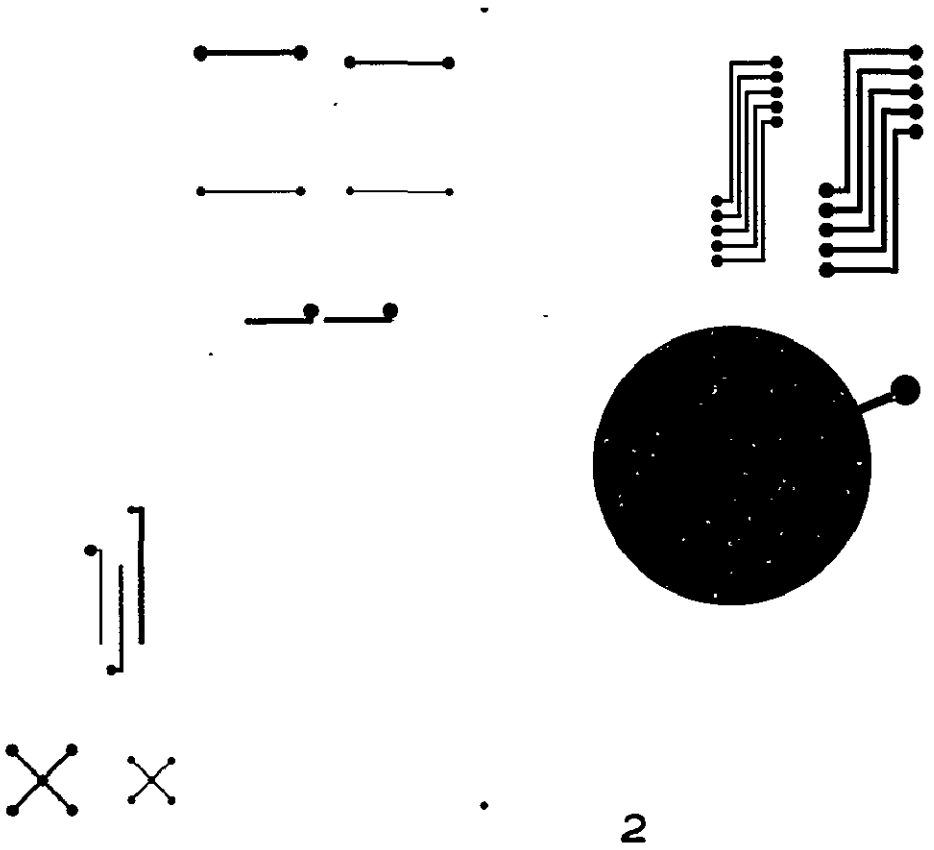


Figure 5. Circuit Pattern 2 of Artwork

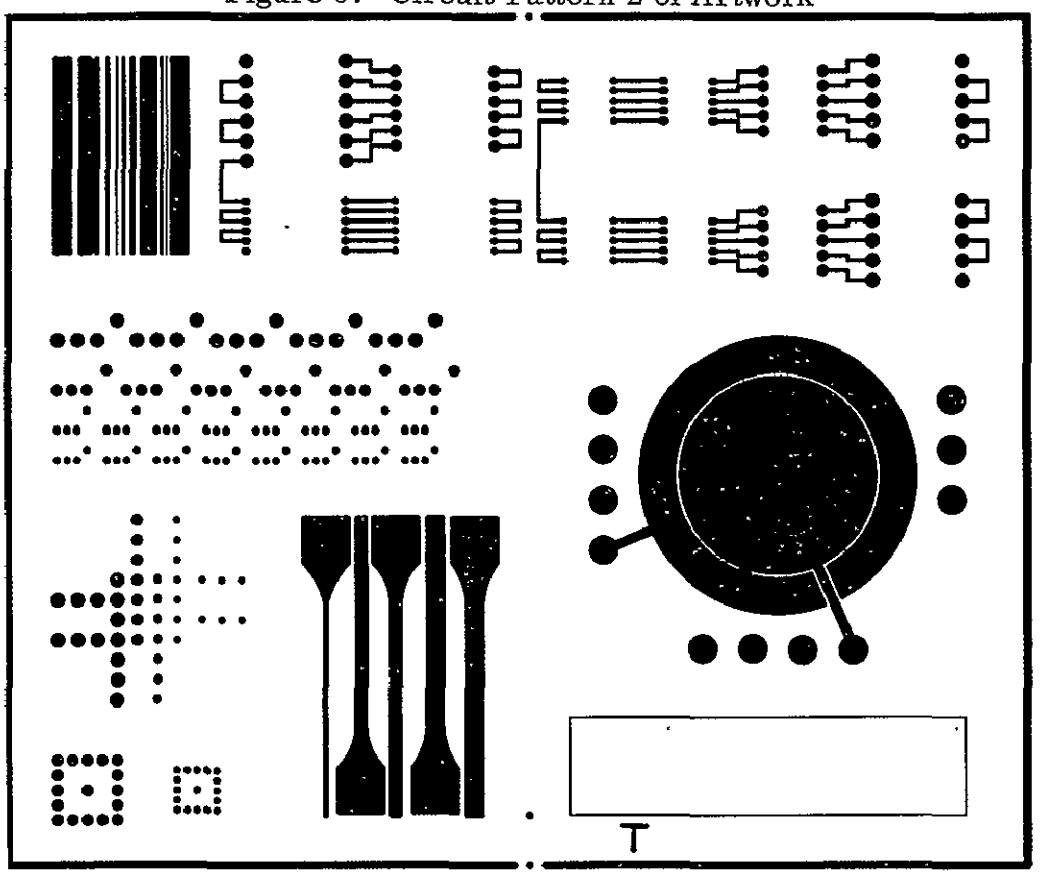


Figure 6. Top Circuit Pattern "T" of Artwork

PYRE ML) at a weight ratio of approximately 90 percent gold to 10 percent varnish. The selection of the varnish was a natural choice since it was the same material used for the dielectric. Thus maximum compatibility of materials was assured as well as utilization of a conveniently built-in molecular interlocking process between binder and surrounding dielectric.

Organic Composites

Tetracyanoquinodimethan (TCNQ) Charge Transfer Complexes. — Several TCNQ complexes with polymeric materials containing electron donors had been prepared and examined during the preceding phase of this program.

A reexamination of electrical resistivities of these complexes with poly-(2-vinylpyridine) indicated that the simple salts (e.g., TCNQ-PVP-1, Ref 1) are stable after several weeks' standing while the complex salts (e.g., TCNQ-PVP-3) suffer a substantial (100X) increase in resistivity in the same time period. Unfortunately it was the complex salts that had the useful conductivities, as experimentally confirmed previously. Evidently the uncharged moiety of these complexes ($TCNQ^{o}$) was only loosely bound and readily lost to, or degraded by, the ambient atmosphere. With it went the conductivity. Some consideration was given to the possible use of the black residues obtained on pyrolysis of the TCNQ complexes in a thermal treatment equivalent to the polyimide cure cycle. However, widely varying weight losses (up to as high as 91 percent) had been previously observed under these conditions (Ref 1) which would have presented serious outgassing problems under repeated polyimide cure cycles and possibly under environmental thermal cycling. It was decided that the TCNQ complexes deserved further attention only if some means could be found (or proposed) for stabilizing their compositions.

Pyrolyzed Polyacrylonitrile (PPAN). — Carrying forward from earlier work (Ref 1), reinvestigation of the pyrolysis of polyacrylonitrile (PAN) was initiated using a differential thermal analysis (DTA) approach. A first run revealed no significant exo- or endothermic peaks up to a pyrolysis temperature of 400 deg C in ordinary air. Although the possibility existed that any thermal excursion associated with the drastic molecular transformation might be masked by operational parameters, it was not considered unlikely that such an effect might be spread over a large range of temperature and therefore be difficult to detect. This expectation has some precedent in the uniform distribution of pyrolyzate resistivities from 10^{10} to 10^{1} ohm cm as a function of pyrolysis temperature over the range 650 to 950 deg C (Ref 2). It was considered important, however, to be fully aware of any existing or potential thermal anomalies before adopting (PAN) in a board fabrication process requiring multiple polyimide cure cycles at elevated temperature.

After some instrumental adjustments continued investigation of the pyrolysis of polyacrylonitrile by DTA revealed a number of exotherms depending on sample preparation and container. The relevant data are given in Table I.

Variations in method are capable of influencing the rate of diffusion of oxygen to the polymer and the rate of heat loss from it. This is reflected in the data, which also indicate the pyrolysis to be a complex process. The main conclusions to be drawn were that things start to happen well below the usual polyimide cure temperature of 315 to 345 deg C and were still occurring as high as 650 deg C.

TABLE I
DTA ANALYSIS OF PAN PYROLYSIS

% PAN	Inert Diluent	Sample Container	Exotherms* (Deg C)
5	$A\ell_2O_3$	Powder	141-160
50	$A\ell_2O_3$	Powder	204-229; 299-320; 371-382
100	None	Powder	404-421; 430-449; 524-599; 641
100	None	Liquid	191-204; 320-338; 374-379; 385-404
100	None	Liquid	229-235; 249-254; 291-349; 424-471; 516-524; 641-649

*Temperature peaks indicating possible molecular transformations.

At least two exotherms occurred below 345 deg C. The question was, were the molecular transformations represented thereby able to confer sufficient conductivity on the pyrolyzate? A partial answer was obtained by pyrolyzing at several temperatures and measuring the conductivities on compressed pellets. The resulting data are shown in Table II.

TABLE II
PPAN RESISTIVITY DEPENDENCE ON PYROLYSIS TEMPERATURE

Pyrolysis Temperature (Deg C)	Resistivity (Ohm Cm)
274 (6 hours)	2×10^{13}
315	2×10^{11}
345	3×10^{9}

Although it is tempting to try to correlate these conductivities with DTA exotherms, it is obvious that the polyimide cure temperature is inadequate for producing the desired conductivity. However the specimens tested were derived from the raw powder and not from a cast film. In the cast film, interlocking of polymer chains might extend throughout the entire specimen body which could lead to improved intermolecular electron transport and a higher conductivity. Efforts to verify this possibility in subsequent experiments (see following text) were thwarted by the fragility and loss of adhesive bonding of the pyrolyzed films.

Another way to achieve lower resistivity (10 ohm cm has been reported for PPAN) was thought to be through the use of organic additives which were conductive and also oxidative. An example was TCNQ; others were various quinones and sulfur derivatives. The main function here would be to assist in the dehydrogenation of the PAN, producing an effect analogous to a lowering of the temperature regions at which the DTA exothermal peaks occurred. Three such candidates were examined and are listed in Table III along with their compressed pellet resistivity values.

The last named material, anthrone.sulfide, was prepared by a method described by Krikorian (Ref 3). This procedure consisted of refluxing the organic starting material (in this case, anthrone) with sulfur in 1, 2, 4-trichlorobenzene at a

TABLE III
POSSIBLE ADDITIVES FOR IMPROVING
PPAN ELECTRICAL PROPERTIES

Material	Resistivity (ohm cm)
Benzanthrone	4×10^{14}
Dibenzanthrone	2×10^{10}
(Anthrone) S_X	2×10^{6}

temperature of about 213 deg C. This process, which was accompanied by an evolution of hydrogen sulfide, was continued for about eight hours during which time a violet-black slightly soluble product gradually separated out. The material was recovered by filtration, and excess sulfur and solvent were removed by volatilization in a stream of nitrogen. The material was found to be insoluble in most solvents and essentially nonvolatile even under vacuum deposition conditions. Thus it at least met the stability requirements necessary for board processing.

The same process was carried out using benzanthrone and dibenzanthrone as starting materials to produce the corresponding sulfides. The conversion of the benzanthrone was essentially zero; that of the dibenzanthrone was practically quantitative and was conveniently monitored by the evolution of hydrogen sulfide. The product was removed by filtration and purified by solvent extraction followed by vacuum sublimation to remove excess sulfur. It was obtained as a deep blue-black powder having a very slight solubility in DMF (purple solution) but virtually no solubility in most other solvents. Its resistivity had been reported to vary from 10^2 to 10^4 ohm cm, which compares favorably with the most promising TCNQ complexes previously examined without sharing their thermal instabilities.

Another possible approach to the promotion of the catalytic dehydrogenation and cyclization of PAN at moderate temperature was to incorporate a catalyst of the cobalt phthalocyanine type. The catalytic behavior of cobalt phthalocyanine is a matter of record (Ref 4) and probably is associated with electronic states of the cobalt atom as modified by its linkage to the nitrogen atoms of the phthalocyanine structure. Samples of cobalt phthalocyanine were still available from the previous year's work and no new syntheses were required.

Formulations and Application Procedures. — The materials investigations and syntheses of the preceding section and the formulations and application experiments described in the present section were undertaken with one main objective in view. That was to utilize PAN either as its own binder or as a binder for some dispersed phase prior to pyrolysis. In the latter case the dispersed solid was to serve as an organic conductor itself, as a catalyst for assisting the dehydrogenation of PAN, or both. In every case the PAN was expected to become at least partly conductive on pyrolysis to PPAN under conditions compatible with other steps in the board fabrication process. It also was anticipated that these formulations would be applicable to the boards through a silk screen delineated according to Pattern "B" of the artwork (Figure 2).

The usual procedure was to disperse the PAN in a solvent to form a colloidal solution. The solvent initially was dimethylformamide (DMF) which tended to produce somewhat gelatinous media (indicative of a high molecular weight polyacrylonitrile) rather than free-flowing solutions. The PAN mixture then was placed in a ball mill along with the desired solid additive (e.g., dibenzanthrone polysulfide) and ground for several hours. The milling improved fluidity to some extent but not sufficiently to make practicable its use with the silk screen (200 mesh) "B" pattern that had been prepared for use in via filling.

This result led to efforts to improve the solvent system for PAN and to seek alternative techniques of application. In the former case a number of solvent compositions were investigated, and their effects on PAN are listed in Table IV. The only improvement found (over plain DMF) was a mixture of DMF with dimethylsulfoxide (DMSO). The dispersion of PAN in this mixture was film-forming and easily brushable. Solutions in DMF alone were more jelly-like and contractile when spread as a film. Simple addition of DMF until the jelly-character disappeared resulted in a thin liquid with poor physical and spreading properties and a high contraction coefficient on solvent removal. Introduction of DMSO permitted higher PAN concentrations which were less gelatinous and more adhesive than when DMF alone was used.

TABLE IV
BEHAVIOR OF PAN IN VARIOUS SOLVENTS

Solvent	Effect on PAN
Acrylonitrile	None visible
Acetonitrile	Softens slightly
Dimethylformamide (DMF)	Dissolves
Methyl ethyl Ketone (MEK)	None
Ethanol	None
PYRE ML Varnish	None
Acetic Acid (glacial)	None
Methylene chloride	None
Acetone	None
DMF + acetonitrile	None
DMF + ML varnish	None
DMF + acrylonitrile	None
Tetrahydrofuran (THF)	None
Dimethylsulfoxide (DMSO)	Slightly soluble
DMF + THF	Very slightly soluble
DMF + DMSO	Film-forming solution

An alternative to the silk screen procedure was the use of a nichrome mask in which the vias had been delineated by standard photo-etch technique. A dispersion of dibenzanthrone sulfide, prepared as described above, in a medium of PAN and DMF alone was used in the test. The thick, essentially black colored liquid was applied to board Number 7 (on aluminum, with three circuit layers) through the nichrome mask by a squeegee process. The procedure proved more controllable than the

previous attempts with screening. All through-holes so treated were completely filled, and surrounding excess was easily removed after a short drying cycle. The board then was heated in a normal air ambient until a temperature of 345 deg C had been reached and maintained for one hour, thus pyrolyzing the PAN to an insoluble, infusible and presumably conductive state. The black deposits thus obtained appeared to be moderately adherent and resistant to abrasion. Electrical (probe) tests disclosed, however, that they were extremely poor conductors and unsuitable for the intended use. Concurrently it was observed that the original ball-milled dispersion had, in the course of a few days, coagulated and lost its original physical properties indicating a fundamental instability of the system and a short shelf-life.

The above result clearly indicated that the anticipated catalysis of PAN dehydrogenation and cyclization by the dibenzanthrone sulfide was not obtained. It was evident from the literature (Ref 5) that both dehydrogenation and cyclization had to occur during high temperature pyrolysis to yield a conductive product. But up to this point it had been assumed (incorrectly) that both effects would occur contiguously, if not simultaneously, under essentially similar pyrolysis conditions.

The dehydrogenation (although not necessarily cyclization) of organic substances can be assisted by oxidants, such as sulfur, TCNQ, etc., and by catalysts, such as cobalt phthalocyanine (Ref 4). Since PAN alone (and with added dibenzanthrone sulfide), when pyrolyzed at the cure temperature of the polyimide, did not yield a sufficiently conductive product, it seemed reasonable to continue the search for a catalytic process that would effectively duplicate at 345 deg C results obtainable otherwise only at much higher temperatures. It was known from other sources (Ref 6) that increasing the pyrolysis temperature increased the conductivity of the PPAN. The boards, however, were not expected to survive the temperature extremes required according to available references; hence the catalytic approach.

Several mixtures were prepared as listed in Table V, the intention being that the PAN in every case would act as a conductive binder after pyrolysis. Each mixture was formulated with a DMSO-DMF solvent. The specimens then were painted on polished aluminum plates and allowed to dry. This was followed by pyrolysis in air at 345 deg C for one hour. It is clear from the results that the additives were ineffective in causing all results expected of a higher temperature treatment even though dehydrogenation might have been substantially accelerated. It also would appear that the intrinsic conductive properties of the additives themselves contributed little (except in the second composition listed) to the electrical properties found.

These results suggested that cyclization (aromatization), which gives rise to electron delocalization, had not occurred to any great extent. Therefore additional PAN samples were prepared, one plain, one with added sulfur and one with added cobalt phthalocyanine, and pyrolyzed in air at 830 deg C for 20 minutes.

This treatment completely destroyed the first two samples and in the case of the third sample, left a black residue only half the weight of the original specimen. This turned out to be electrically conductive, but further examination led to the conclusion that the powder was mainly cobalt oxide and contained little or no organic residue.

TABLE V
CATALYSIS OF PAN PYROLYSIS

Additive	PAN/Additive Ratio (w/w)	Specimen Resistance
Cobalt Phthalocyanine [a]	10:1	Nonconductive [b]
Cobalt Phthalocyanine [c]	1:10	3×10^5 ohms
Co/Mn Phthalocyanine	1:10	Nonconductive
TCNQ-PVP-2 [d]	1:1	Nonconductive
Cobalt Phthalocyanine [a]	1:10	Nonconductive
Co Phthalocyanine [a] + Sulfur	1:10	Nonconductive

[a] Purified sublimate (Ref 1)

[b] As measured by VOM on a film approximately 0.001 in. thick after pyrolysis

[c] Unpurified, suspected of containing some cobalt oxide

[d] Previously prepared complex (Ref 1)

The sequence was repeated at a temperature of 660 deg C with similar results, the samples lacking cobalt phythalocyanine disappearing completely. It was concluded that molecular cyclization could not proceed rapidly enough to offer, through ladder-type structure, protection from oxidative attack. This led to the further idea, however, that cyclization would occur independently of dehydrogenation and only at relatively high temperatures where the vibrational energy levels of the molecules would provide a high probability (and therefore rate) of ring closure. Furthermore, the effects of catalysts and oxidants would be negligible even though they might assist in the dehydrogenation at lower temperatures.

Another set of three PAN samples was prepared and vacuum baked 30 minutes at 900 deg C and at a pressure of 50 microns. During the process both sulfur and cobalt phthalocyanine were outgassed from the samples so treated. Black residues were obtained in every case, accompanied by substantial weight losses. All were conductive, with thin-layer resistances of two to five ohms in every case, as measured with a VOM. The initial presence of additives appeared to have no effect whatever on the final electrical characteristics.

The results tended to confirm the mechanism postulated above and led to the development of a standard PPAN preparation. This involved heating PAN in air at 345 deg C for 1.5 hours (weight loss about 35 percent) followed by a 30 minute vacuum treatment at 900 deg C (weight loss about 75 percent; total loss, 83 percent). The high temperature weight loss probably resulted from the action of residual oxygen in the vacuum chamber.

PPAN produced as above was formulated with fresh PAN (to act as binder) and solvent in a ball mill, after which it was applied to existing vias in Board 9 (on aluminum, with three circuit layers). which had been previously delineated with a nichrome mask. Curing was carried out at 345 deg C for one hour. The resulting vias were found to be electrically conductive. Adhesion to the gold metallization, however, was faulty and gave rise to mechanical flaking during electrical probing.

Instead of fresh PAN, polyimide varnish was used in a following experiment. This was applied initially to a polished aluminum planchet and cured in the usual manner. The resulting layer exhibited good electrical conductivity (with a bulk resistivity estimated at 10 ohm cm, or less) and good adhesion. Adhesion to gold remained to be determined but, at the very least, the possibility existed of establishing a strong chemical bond between the polyimide binder and the surrounding B-stage polyimide dielectric.

The foregoing investigation essentially determined the z-direction organic conductor and eliminated from further consideration other conductors of organic origin previously considered. It should be emphasized that the thermal treatments employed in making the PPAN did not produce graphitic material. The repeating molecular unit is not the six-carbon-atom benzene ring characteristic of graphite but the heterocyclic five-carbon-atom, one-nitrogen-atom, pyridine nucleus (Ref 1). Furthermore, the temperatures required to produce graphitic material are of the order of 2000 deg C and higher (Ref 7) which exceeds by a considerable range the temperatures employed here.

The results of this investigation also tended to confirm the validity of the structural considerations adopted in an earlier phase of this program (Ref 1) and the selection, at that time, of PPAN as one of the four classes of organic materials that might yield useful conductors.

The polyimide/PPAN organic conductor adhered well to the aluminum substrate after curing but less well to a gold substrate on Board 10. The very large diameter vias surrounding the capacitor were particularly prone to adherence failure after cure at 345 deg C. In addition, film cracking, apparently due to shrinkage, was noted in all cases of poor adhesion. The application procedure therefore was modified by removal of loose material and reapplication of fresh conductor mixture. The second cure was limited to 275 deg C. This dual treatment yielded intact z-direction conductors having good mechanical stability. Continued attention was devoted to the organic conductor throughout process development to ensure its compatibility with the various treatments used and to modify or improve the application technique as required.

BOARD FABRICATION

Procedures and Sequence

The procedures utilized in board fabrication were developed in detail in the first period of this program (Ref 1) but only a beginning had then been made in fitting them together into a coherent process. In creating a successful process it was

necessary from time to time to introduce, remove or modify process steps. Major process steps, therefore, will be dealt with in general terms but modifications will be described in detail. The major steps are considered below.

Step 1. Polyimide Base Layer. – The polymide varnish (duPont "PYRE ML", referred to in the following sections as "ML varnish" or "varnish") was applied without dilution as received from the manufacturer. It was stored under refrigeration (manufacturer's recommendation) but was allowed to come to room temperature before application in order to avoid viscosity-dependent variations in film thickness. It has a consistency and color similar to molasses. The most successful technique of application was to cover the entire board with a layer of varnish, then spin off the excess as normally done in photoresist applications. Tools and equipment were easily cleaned with DMF. Spinning speed-and-duration was adjusted according to the equipment used and in the direction of achieving maximum film thickness without sacrifice of uniformity. Film thicknesses so obtained were 150 to 200 microinches after cure. After initial solvent evaporation at room temperature (about 30 min) a cure to b-stage at 85 deg C (20 to 40 min) was applied. At this stage the film could be masked and etched prior to final cure. For the final cure temperature was advanced 2.0 to 2.5 deg per minute to a level of 315 to 345 deg C which was maintained for one hour. For Step 1 no vias were required and the base layer was carried directly into final cure without isolation at the b-stage. This step was applied to both Vespel and aluminum boards. Although not required for electrical isolation on the Vespel substrates it had the effect of partly smoothing out the milling marks and of providing a foundation layer of unvarying properties. In a later modification double applications were used to increase the layer thickness (to approximately 250 microinches).

Step 2. Circuit Layer Number 5. – Metallizations were vacuum deposited at 10^{-6} Torr from metal granules fed into a flash evaporation source. For maximum adhesion a nichrome flash was first applied followed by a gold deposition in the range of 0.9 to 1.2 microns thick. Riston photopolymer then was laminated to the gold surface, exposed through the artwork ("Number 5", Figure 1) and developed. Etching of the gold layer was accomplished with iodine-potassium iodide solution (hereinafter referred to as "KI_3 solution")* and the nichrome, with ceric sulfate solution.** The remaining Riston was removed with stripping solvent (methylene chloride). Visual inspection was made for delineation flaws and line continuity.

Step 3. Polyimide, b-stage.- Immediately prior to the second varnish application the surface of the board was moistened with DMF and allowed to "soak" for two to three minutes. The solvent was allowed to evaporate off (or spun dry) after which the varnish was applied exactly as in Step 1, but cured only to the b-stage.

Step 4. Copper Mask, B-1; Etch. - A copper layer*** was vacuum deposited on the b-stage polymer and Riston photopolymer laminated to the copper surface. This was followed by exposure through the via artwork (B-1) and development. The copper layer was etched (usually with ferric chloride solution) through the Riston mask, followed by careful rinsing. The vias then were etched in the b-stage polyimide layer with ammonia solution (concentrated ammonium hydroxide diluted with 20 volumes of

*Formulation: 225 g potassium iodide, 75 g iodine and 132 g dibasic ammonium phosphate in one liter of water.

**Formulation: 50 g ceric sulfate in one liter 10% nitric acid.

***For masking purposes copper layers were 6000 to 8000 Å thick.

deionized water) without first removing the Riston mask. The double mask (Riston/copper) served as a valuable precautionary measure in preventing occasional diffusion of the ammonia to b-stage polymer where it was not desired. (This was later confirmed by dielectric defect density measurements in the large capacitor areas). Via etching usually was complete in about one minute and seldom required mechanical assistance. The etched vias were permitted to "bleed" slightly in order to cover the exposed gold pads with an extremely thin polyimide film. After drying the surface in a jet of nitrogen the Riston mask was removed with stripping solvent. The board was now ready for Step 5. If Step 5 (via filling) was to be omitted the copper mask also was stripped off and the board freed of etch residues by thorough rinsing. (Deionized, or distilled, water was specified in all solutions used). Curing then was completed at 315 to 345 deg C as specified in Step 1 and the board was advanced to Step 6.

Step 5. Fill Through-Holes. – Through-holes, or vias, were filled individually by hand using a thin glass rod, or similar instrument, as an applicator. This admittedly slow and painstaking process grew from the current absence (but not technical unfeasibility) of a multiple filling process that yielded reproducible results. The conductor materials applied were gold-filled or PPAN-filled ML varnish, as specified in the previous section. Misapplied material was easily cleaned off the copper mask with the aid of DMF. After filling, the board was subjected to a b-stage cure cycle as specified in Step 1. The copper mask was then stripped off and the board thoroughly rinsed. The cure cycle was completed as in Step 1. The z-direction conductor applications were visually examined for flaws and corrected where necessary with additional spotting of conductor mixture. If this was done, an additional cure cycle was applied terminating at 300 to 315 deg C.

Steps 6, 10 and 14, Circuit Layers. – These steps were identical with Step 2 but employed artwork negatives 4, 3 and 2 (Figures 3, 4 and 5) respectively.

Steps 7, 11 and 15, Polyimide, b-Stage. – These steps were duplications of Step 3.

Steps 8, 12 and 16, Copper Masking and Etching. – These steps repeated Step 4 but with artwork negatives B-2, B-3 and B-4 (See Figures 7 through 10) respectively. This set of via patterns represents a modification of the original via artwork ("B", Figure 2) and was introduced for reasons described in the following section.

Steps 9, 13 and 17, Fill Through-Holes. – These steps duplicated Step 5, but as a result of process modifications all but the final filling, Step 17, were eliminated.

Step 18. Nichrome/Copper Deposit. – A contractual requirement (Item 5, Statement of Work) called for solderability of components to the exposed top layer. This step, therefore, was a duplication of Step 2 except that copper was substituted for gold.

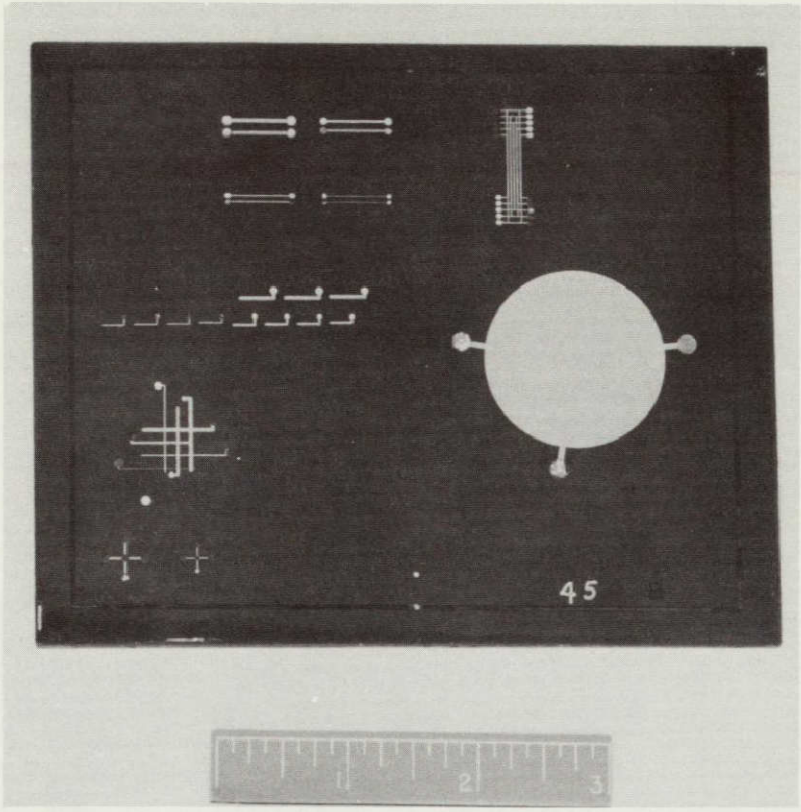


Figure 7. Board 10 Vespel, After Step 8

Step 19. Tin-Plate, "T" Pattern. – Riston was laminated to the copper surface produced in Step 18 and exposed through Pattern "T" of the artwork. The photopolymer was developed to define the "T" pattern in exposed copper. The back and edges of the board then were masked with protection tape. The board was placed in an electrolytic cell with electrical connection to the copper layer and tin-plated. After rinsing, the residual Riston was stripped off.

Step 20. Final Etch. – The "T" pattern, delineated in tin-plate in the preceding step, served as a mask for the etch removal of exposed copper and nichrome using ferric chloride and ceric sulfate solutions respectively. The only material exposed to the ambient by this process was the underlying, fully cured polyimide film; all internal gold metallizations were completely protected. The board was rinsed to remove etch residues, which completed the fabrication.

Figures 7, 8, 9 and 10 show boards at various stages of completion. Figure 7 shows a board, (Number 10, Vespel substrate) after Step 8 with the first two circuits. Figure 8 shows a board after completion of Step 12 (Number 27, aluminum substrate) and having three circuit layers. A board after Step 16 (Number 23, aluminum substrate) is shown in Figure 9 and has four circuit layers. Figure 10 shows a completed board (Number 37, aluminum substrate) with five circuit layers, the top layer being exposed to the environment and making electrical connection with the z-direction conductors which communicate with underlying circuit levels. Two of the incomplete boards displayed certain anomalies, some of which are visible, and and were dropped from further processing (see following text).

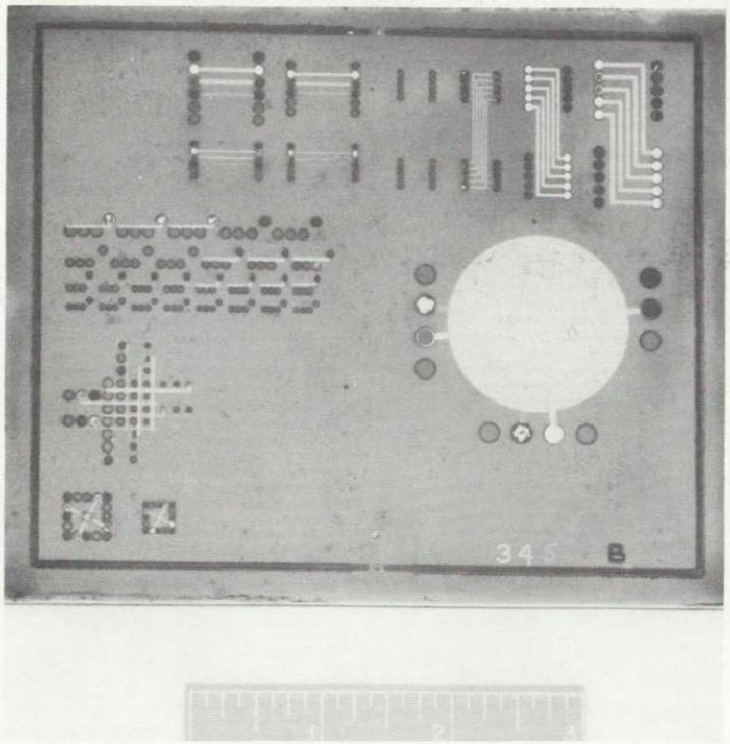


Figure 8. Board 27 on Aluminum, After Step 12

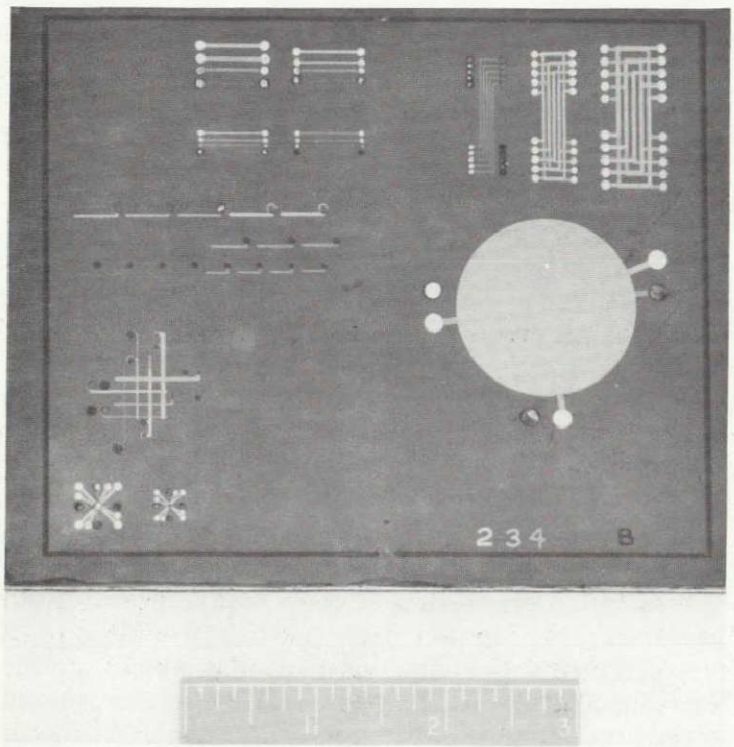


Figure 9. Board 23 on Aluminum, After Step 16

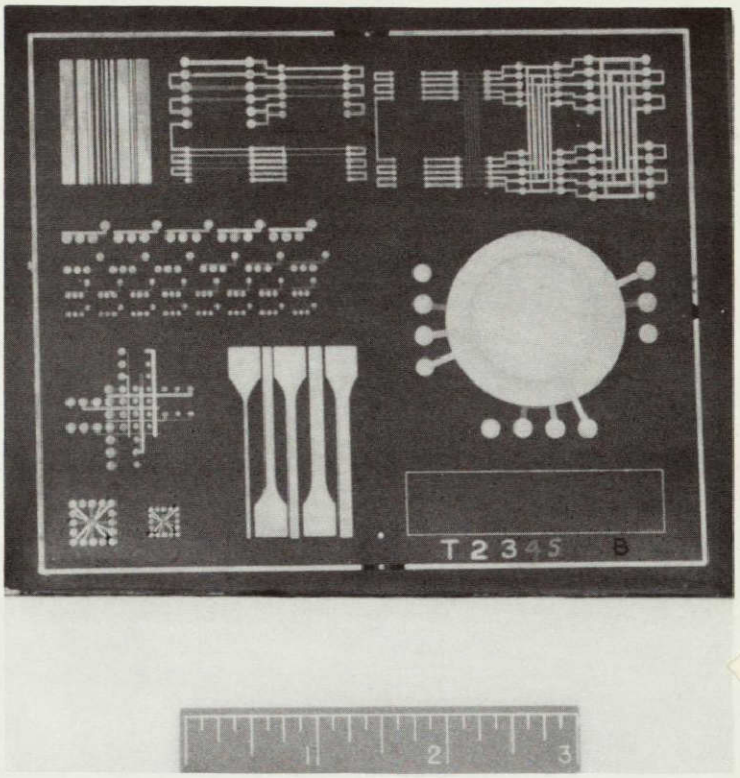


Figure 10. Board 37 on Aluminum, After Step 20

The above process step designations were utilized in abbreviated standard format throughout most of the program for periodic reporting of fabrication progress. The format is displayed in a later section (Table VII) which summarizes this progress for the entire period.

Process Modifications and Refinements

Process modifications were made either through necessity, to achieve compatibility with other board treatments, or for reasons of obvious improvement in such areas as fabrication reliability (yield), labor cost or meeting the completion schedule. These modifications are considered individually below. Their incorporation in the preceding processing sequence is to be assumed where not specifically designated.

Blistering in Gold Metallizations. – Incautious advances in cure temperature of a polyimide layer was blamed for occasional lifting of gold metallizations mainly in the large capacitor area. A flagrant example of this effect is shown in Figure 11 (Board 17 on Vespel after Step 12) following cure of a newly etched polyimide layer. A less obvious example is shown in Figure 7, also on a Vespel substrate. However, no significant correlation of this failure mode with substrate material could be drawn. A total of seven boards were sacrificed to this cause, four of them on aluminum.

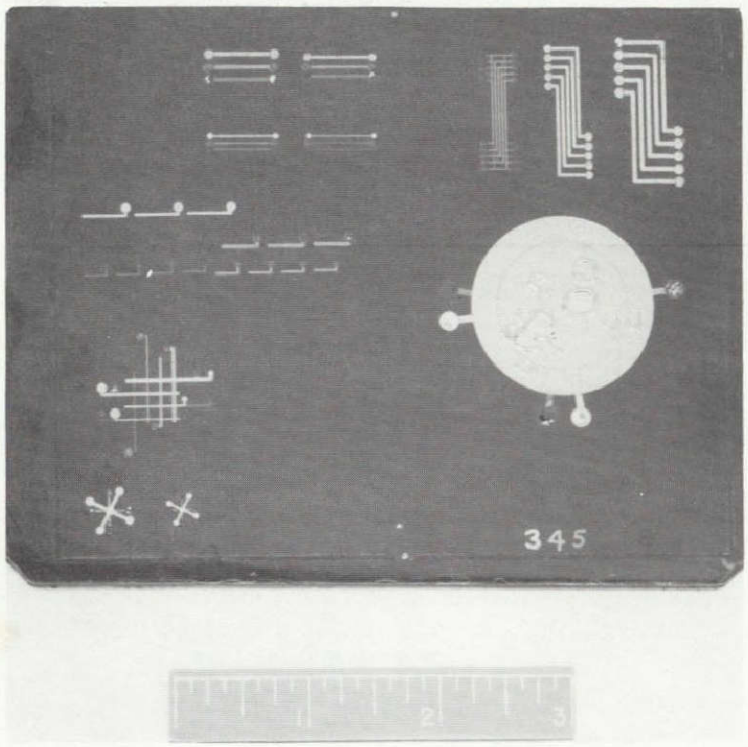


Figure 11. Board 17 on Vespel, After Step 12

Although infrequent, these failures were distributed throughout the manufacturing period and appeared to have no dependence on process modifications introduced in this interim.

A contributing factor to the phenomenon was considered to be the chemical inertness and specular nature of the noble-metal areas which provided a poor footing for adhesive bonding to the contiguous polyimide layers. A second, but much more remote, factor may have been ammonia penetration under the gold during the preceding etching step. This would have required substantial penetration of the ammonia through several layers (Riston/copper mask, green polyimide and the gold layer) during the same time (one minute) it took to etch the exposed vias. The occurrence of the blistering itself tends to refute the possibility of a porosity in the metallization sufficient to admit the ammonia in the first place. A more likely possibility is the action of steam generation, either from water absorption over an extended period, or from an incompletely cured underlying polyimide layer.

The process modification in this case consisted simply of giving closer attention to cure schedules and of guarding against the omission of final cures.

Adhesion of Nichrome Residues. – Vacuum deposited nichrome was employed in two ways: on fully cured polyimide as an anchor for a succeeding gold deposition and, for a time, on b-stage polyimide as a via mask. The latter application gave rise to cure cycle problems which are discussed in the accompanying text. In the former

case nichrome residues occasionally were observed to resist all attempts at etch removal. These residues appeared as dark blemish areas which stained the incorporated polyimide layers, but probably would contribute nothing to electrical malfunction.

The problem was last encountered with Boards 19, 20 and 21 (on aluminum) at Step 20. Etching attempts, accompanied by mild mechanical abrasion, caused damage to the "T" layer and the boards had to be recycled back to Step 18. At the same time investigation was made into probable causes of the etching failure. Of prominent concern was the possible presence of passivation oxide layers on the nichrome layers that might prevent penetration and oxidation of the metal by the ceric ions. Pretreatment of the nichrome layer by a strongly acting reducing agent therefore was investigated. This was a solution of stannous chloride (9 to 10 percent by weight) in concentrated hydrocholoric acid. This treatment was found to be highly effective in assuring the complete removal of ceric sulfate in the subsequent etching step. Conversely, application of the ceric sulfate first tended to carry the passivation to a more refractory state and rendered the stannous chloride solution ineffectual.

The process modification consisted of limiting the density of the nichrome flash and of applying a hydrochloric acid solution of stannous chloride immediately prior to ceric sulfate etching. After these changes no further difficulties were encountered.

Polyimide Cure, Anomalous. —Irreversible adhesion of nichrome residues also was observed in its use as a via mask (see foregoing discussion) on b-stage polymer. A coincident observation was the excessive resistance of the "b-stage" polymer to via etching, a problem particularly acute on Vespel boards. The known poor heat transfer characteristics of the Vespel substrates (not shared by aluminum substrates) and the necessarily high thermal energy of the vaporized nickel and chromium atoms led to the hypothesis that a transient overheating had carried the polyimide cure well beyond the b-stage. All visual and tactile evidence was in support of this hypothesis.

Remedies were sought initially in modifications in polyimide etch compositions to include either a stronger base or a solvent additive that would increase the "effective basicity" of the ammonia. (Ammonia was preferred because of its automatic elemination by volatilization in the subsequent cure cycle). These solutions, however, still required the assistance of mechanical abrasion in the clearing of vias and could not be utilized in a practical fashion.

Another approach, deliberate under-curing of the b-stage polymer to "compensate" the expected thermal excursions, likewise did not avail in solving the difficulty.

A successful remedy was found only in the substitution of a lower thermal energy deposit for the nichrome, in this case, copper.* This substitution proved to have a number of advantages. The copper layer resisted alkaline etches; it did not anchor irreversibly to the b-stage polyimide (as had the nichrome); it was capable of sharp etch delineation; it prevented irreversible bonding of the Riston to the underlying b-stage polyimide (which was another problem with the nichrome — note following discussion); it left no visible residue on stripping from the polyimide; and most important, it did not result in curing the polymer beyond b-stage susceptibility to normal etching technique.

*Vacuum deposited, 6000 Å.

Over-cure effects on b-stage polyimide caused by nichrome deposition resulted in the loss of six boards, three on aluminum and three on Vespel. The three on aluminum were considered recoverable and were kept available for possible use.

Over-cure by other means occurred to only one other substrate (Board 5 on aluminum) which inadvertently was exposed to an excessively high cure temperature. Delamination from the substrate occurred as a result and the board was discarded.

Riston Adhesion. – Irreversible adhesion of Riston was encountered under three different sets of circumstances. One of these resulted in the incomplete stripping of Riston from gold metallizations after circuit delineation. The final stripping was done with a methylene chloride base solvent. A search for further information located a "recommended" procedure consisting of rinsing with the following sequence of solvents: used stripper; new stripper; 10 percent methanol in trichlorethylene; isopropanol. Application of this sequence in the removal of Riston from the gold metallization resulted in prompt improvement. In no case was residue in visual evidence, even under ordinary light microscopy. Polarized light microscopy revealed occasional granules but their positive identity could not be ascertained and their cumulative effect in a completed five-layer board was expected to be inconsequential. The sequence therefore was adopted for Riston stripping from circuit metallizations.

At an earlier stage of process development Riston was used by itself on b-stage polyimide as a via mask. Occasionally the under-cured polyimide displayed a tendency to bond irreversibly with the Riston, probably during the laminating step. Some minor alterations in procedure, such as reductions in time or temperature of treatments during and following Riston application, failed to yield conclusive results. Insufficient setting of the Riston resulted in insufficient adherence and loss of fine line definition. Over exposure to uv irradiation, due to variations in procedure, also appeared to be implicated but was considered of minor consequence compared to the possible reactivity of the b-stage polyimide. The problem was temporarily solved by inserting a metallization layer between the Riston and green polymer. This metallization initially consisted of vacuum deposited nichrome. In relatively thick layers it formed a base from which the Riston was easily stripped.

The adoption of a nichrome layer, however, introduced other problems (as previously discussed) which led to other remedial actions, including a thinning of the nichrome layer. The third Riston adhesion problem was associated with the thin nichrome layers. Subsequent experimental investigation showed that the nichrome was porous and could be penetrated by ammonia, which produced a lifting of the nichrome film and subsequently etched away the b-stage polyimide underneath. Thus, if the Riston via mask was left on the nichrome film, ceric sulfate was no longer required for the metal removal. The observed porosity provided an explanation for the adherence of the Riston which probably was anchoring to the underlying polymer through the same pores. Reduction or elimination of the porosity could be achieved with a heavier layer of nichrome but not without risk of further curing the b-stage polymer. The problem was permanently resolved by substituting copper for the nichrome, as noted in the preceding section.

Over-all casualties due solely to irreversible adhesion of Riston totalled only three, one of which was recycled (Board 9 on Vespel).

Dimensional Stability of Vespel Substrates. -- Vespel boards, especially those of 0.06 inches or less in thickness, occasionally displayed a tendency to warp on application and cure of the first varnish layer. Application of a second varnish layer on the reverse side was ineffective, or at best, highly variable, in reversing the distortion. In a number of cases, however, the curvature appeared sufficiently unimportant to permit continued processing. This was done since no adequate remedy or preventive measure seemed available.

It was indeed found possible to apply to slightly distorted boards the various required coatings and to delineate circuit and via patterns without serious misregistration. An unanticipated problem came to light, however, following lamination of Riston to copper-coated b-stage polymer (Step 4). This took the form of localized delamination of the green polymer from the underlying layers and occurred mainly during the via etching step.

The sequence of treatments leading to this deterioration suggested that the lamination step was to blame. In the lamination process, a warped board inevitably will be flexed due to roller pressure. Since the adhesive bond of b-stage polymer to the underlying surface is immature, a potential or latent delamination may ensue even though visible evidence is absent. At a later step, such as etching or curing, the bond weakness and deterioration suddenly become apparent. This was the case with boards 12 and 13 on slightly warped Vespel substrates and also may have been the case with board 10, also slightly bowed, in which some film adhesion in the capacitor area was lost. Processing on these and other warped substrates was abandoned and new starts on Vespel were not continued if visible warping was introduced in the first application and cure of ML varnish. No evidence of subsequent warping was found, even in environmental stressing, if the board survived the first varnish treatment. Losses to this cause totalled four.

Via Etching - Mask Materials. The first and, from a processing point of view, most attractive mask material for via etching was Riston alone. In its use, however, certain difficulties soon materialized, including the irreversible adhesion of Riston to b-stage polymer as referenced above. Another problem was the delicate handling required to prevent loss of fine detail, particularly during inoculation with z-direction conductor. This problem was aggravated by the strong solvent action on the Riston by the DMF contained in the z-direction formulation. As a result this approach had to be abandoned.

In a following modification a nichrome layer was deposited on the b-stage polyimide prior to Riston lamination. The via pattern was defined by the Riston mask and etched in the nichrome layer with ceric sulfate. The vias then were etched in the polyimide layer followed by removal of the Riston. The nichrome mask considerably facilitated the application of z-direction conductors. Its use, however, introduced new problems. To make the process work it was necessary to strike a fine balance between depositing too much nichrome, which tended to bond permanently to the b-stage layer and over-cure it (see Steps 4 and 5), and too little nichrome, which was porous and gave rise to irreversible Riston bonding.

The third procedure, which utilized copper instead of nichrome as the metallization, adequately resolved these problems.

Via Etching - Metallization Protection. An initially unsuspected consequence of adapting artwork from a drilled-hole type of technology to a layer-by-layer process was the lack of circuit mask protection afforded certain pre-existing vias which were not intended to make electrical contact at a given circuit level. The via pattern initially used contained all the vias (Via Pattern "B", Figure 2). It was quickly recognized that a given circuit pattern would cover only the vias pertinent to that pattern while leaving the rest exposed to etchant attack during circuit delineation. It was essential, therefore, that inoculation of z-direction conductor be made at each of Steps 5, 9 and 13 (as well as 17) to prevent this attack.

Although this approach was adopted it eventually proved impractical because of the temporary lack of a completely reliable squeegee process or other multiple inoculation technique. An alternative procedure therefore was introduced in which via walls were permitted to "bleed" slightly after etching, thereby extending a very thin polymer film across the gold pad. The film thus formed subsequently would be fully cured, and even thickened in further processing, but would protect the gold from etchant penetration. Prior to z-direction conductor application the protective polyimide film would be removed with the aid of alkaline reagents. Concentrated aqueous ammonia appeared to be effective in this regard, assisted by mechanical or air-jet action.

Subsequent experience proved, however, that the polyimide films were extremely etch resistant. Mechanical probing sometimes was successful in assisting polymer removal but occasionally resulted in damage to gold pads and shorting to the aluminum substrate. A new etching procedure therefore was devised consisting of a ten-minute treatment of saturated sodium hydroxide solution at 200 deg C. This was followed by a water rinse to remove the sodium salts and an acid rinse to ensure complete sodium removal. The procedure could be repeated in cases where removal was initially incomplete. The gold pads remained intact under these treatments by which they were readied for the final z-direction conductor application (Step 17).

Via Patterns. – Two modifications in via masks were made, the first, and most important, being the elimination of unused vias by restricting the B-patterns only to previously exposed gold pads. This change was initiated not only to simplify z-direction conductor application but also to solve a more serious problem: the loss of fine-line gold conductor continuity at the edges of via wells etched in the b-stage polyimide. Although the discontinuities in level at these "steps" were only of the order of 0.002 to 0.004 in., they appeared sufficient to weaken the adhesion of Riston photopolymer patterns and render them vulnerable to etch under-cut, particularly in the case of fine lines.

A review of previous electrical tests on partially completed boards provided some confirmation of this effect. That is, electrical continuity was found to be significantly greater on the first circuit layer (No. 5) than on succeeding layers, apparently because no drops in level were involved. The possibility of this problem was not considered earlier because it was initially planned to fill in all vias with z-direction conductor after each via etch. So far, however, this has proved impractical. The new set of No. B masks (designated B-1 through B-4, Figures 12, 13, 14 and 15) solved the problem by effectively eliminating all step-downs in gold conductors.

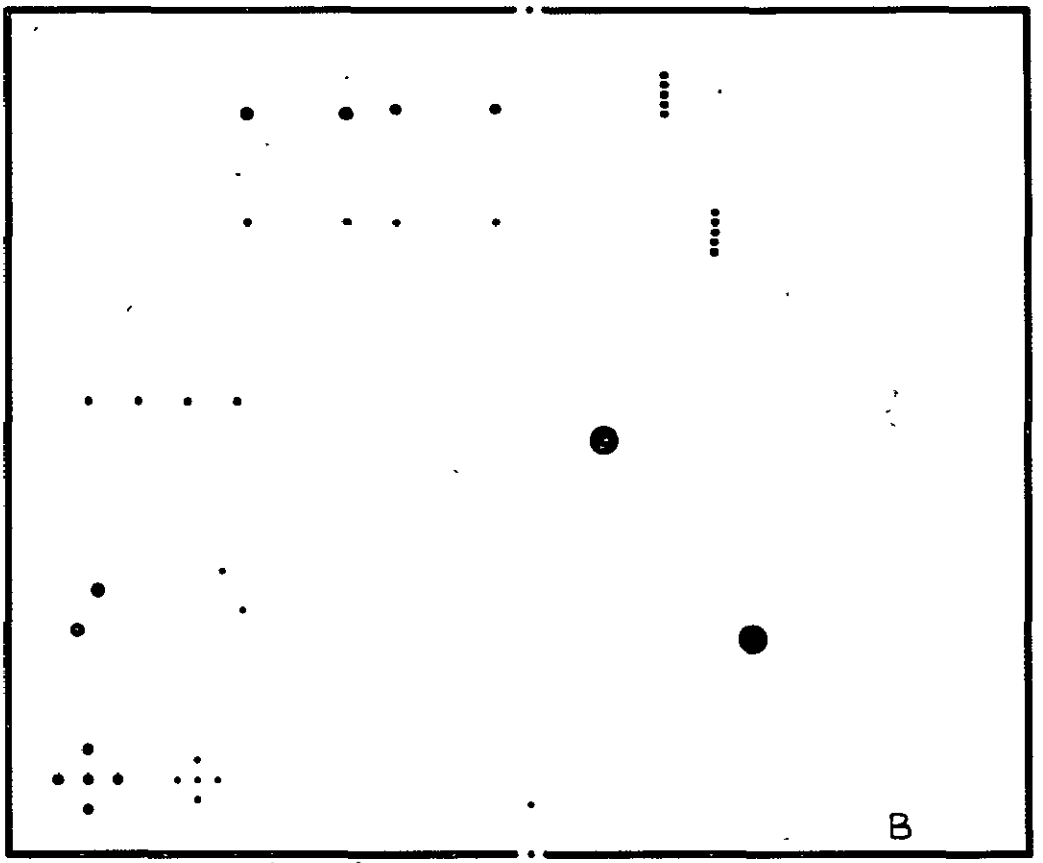


Figure 12. Modified Via Pattern B-1

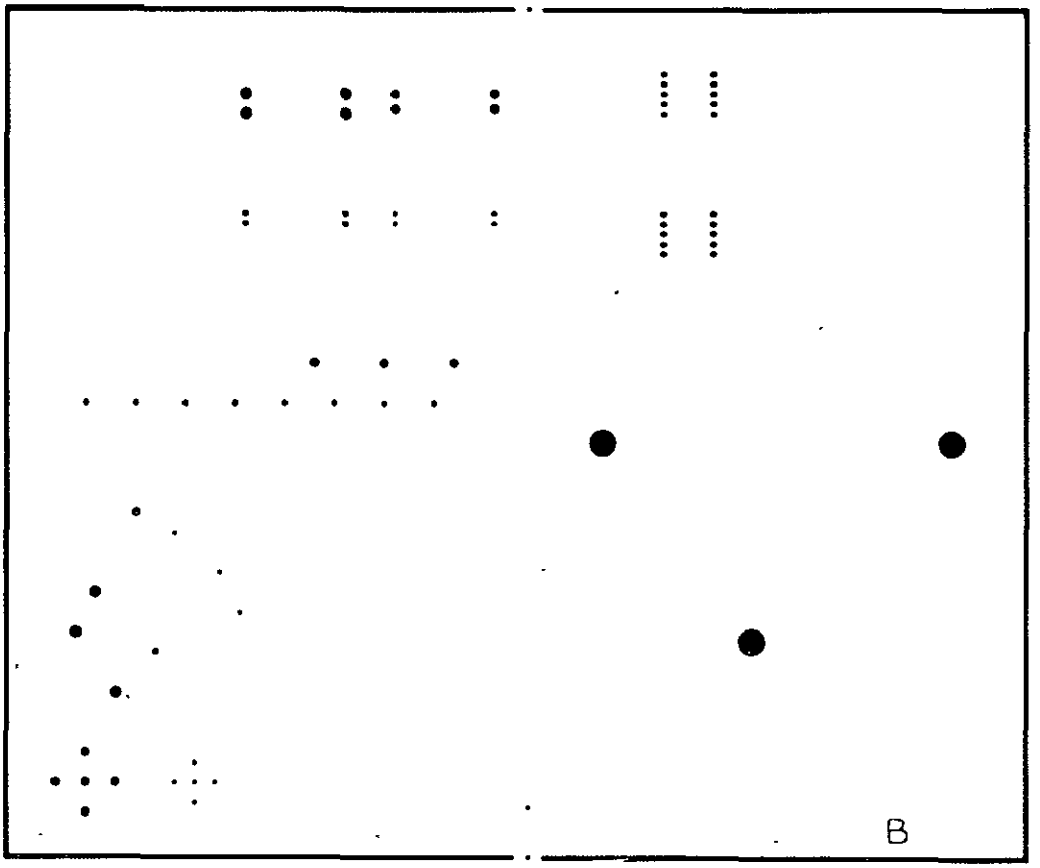


Figure 13. Modified Via Pattern B-2

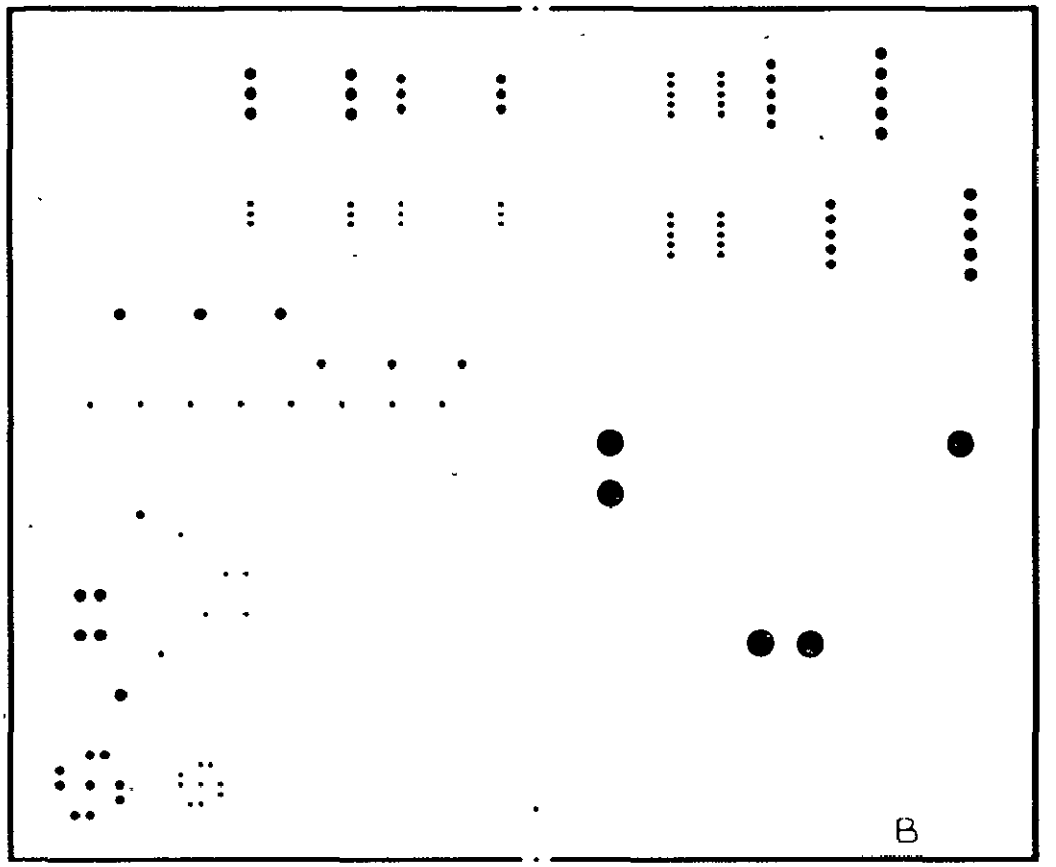


Figure 14. Modified Via Pattern B-3

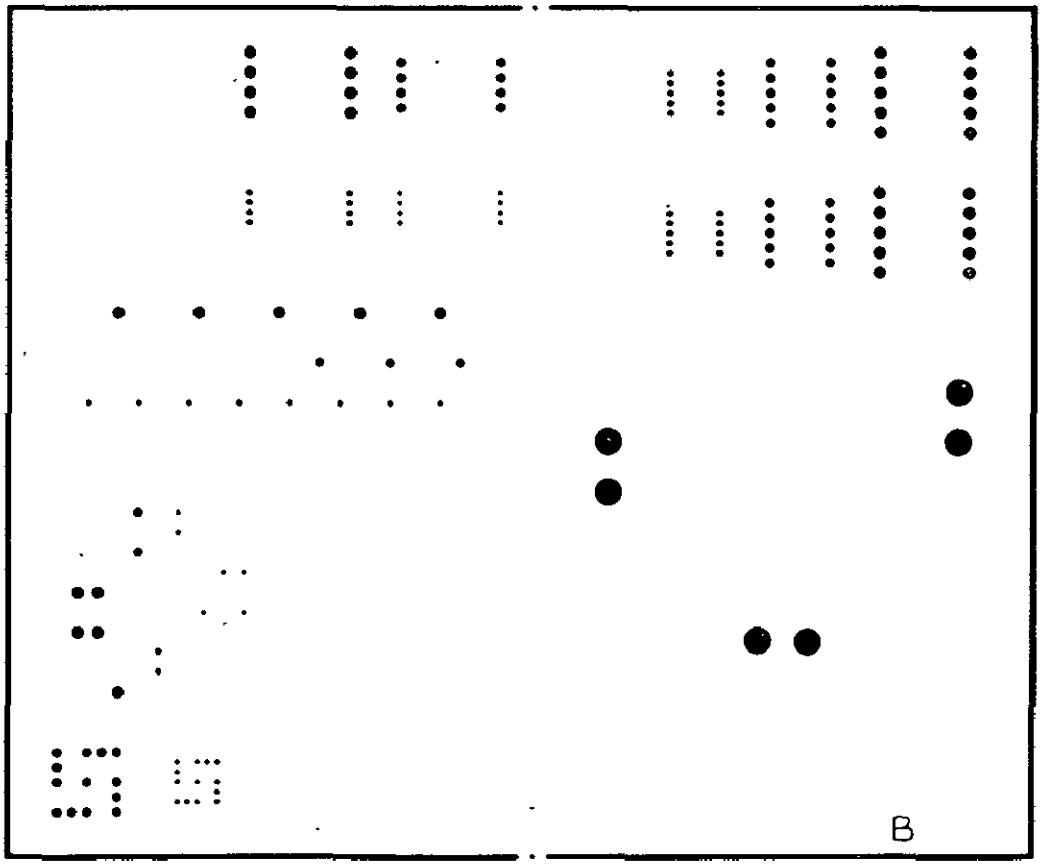


Figure 15. Modified Via Pattern B-4

Diameters of via patterns in the No. B masks also were reduced by about 0.006 inches to improve electrical isolation between closely spaced z-direction conductors. In the ammonia etching of b-stage polymer it is difficult to prevent lateral penetration. Thin walls are thus rendered partly fluid, and the artwork should be designed with this possibility in mind. An acid stop-bath also improved process control.

The discarding of "step-wise" applications of z-direction conductors described in the preceding section, and the changes in via artwork indicated above, were introduced concurrently as process modifications and assisted materially in expediting board fabrication and in improving ultimate electrical reliability.

Via Etching – Reagent Quality. – A somewhat elusive problem for a time was the intermittent occurrence of a tenacious etch resistance in the b-stage polyimide. This problem was experienced one or more times by each of three technologists employed in the fabrication program. At first the occurrence of this effect was laid to a lack of appropriate control of substrate temperature and/or duration of treatment during vacuum deposition of nichrome, then in use as a masking material for via etching. However, the sporadic occurrence of etch resistance remained essentially unchanged in frequency while the nichrome deposit was being deliberately altered in the direction of increasing thinness to eliminate polyimide over-cure. Furthermore, if over-cure were the cause of etch resistance a stronger base, such as sodium hydroxide, should have succeeded where the ammonia had failed. The polymer residues in question, however, were found to be relatively indifferent even to sodium hydroxide.

The true nature of the problem was perceived eventually to be one of ion exchange. To understand it correctly it was necessary to follow the b-stage polymer from a slightly altered point of view through the etching procedure, consisting of immersing the board in an aqueous ammonia solution, rinsing off with water and drying in a jet of air or nitrogen. The board was then visually examined for completeness of removal of polymer from via wells. If residues were present it was frequently found that no amount of additional ammonia treatments would avail in their removal and, indeed, sometimes seemed further to toughen the residues. But the residues in many cases could be (and occasionally were) lifted out mechanically because the polymer had undergone a weakening in mechanical properties by the treatment. When conditions were favorable, however, one or two ammonia treatments sufficed to remove all of the b-stage polymer from the vias.

The b-stage polymer can be regarded as a polycarboxylic acid bound to a long organic chain, that is, a soap-former. Addition of sodium hydroxide, or any other monovalent base (e.g., ammonia), will convert the b-stage polymer to a soap-like product that is soluble in water. But polyvalent ions convert it into an insoluble product, just as ordinary soaps behave in hard water containing calcium, magnesium and ferric ions. Once the insoluble product is formed it strongly resists redissolution because the polyvalent cations hold tenaciously to the carboxyl groups. B-stage polymer insolubilization by polyvalent ions proved to be the key to the problem.

The corrective action taken was to ensure that accidental inoculation with polyvalent ions (e.g., from a contaminated water supply) was avoided in the make-up of solutions and rinsing of boards, and that where such inoculation was suspected (e.g., from weakly acidic etch solutions) the boards were first rinsed in acid before the ammonia etch. In the latter category tetravalent ceric ions used in nichrome

etching were considered especially harmful, particularly on prolonged contact. Adoption of the above measures resulted in immediate improvement and via etching became 100 percent effective.

Top Conductor Layer – Composition and Procedure. – The additional requirements of the "T" circuit layer, namely, that it be exposed to the ambient atmosphere and that it be capable of accepting solder connections, necessitated a metal composite different from that used in the four underlying circuits. These composites started with a nichrome/copper deposition which was to receive a final protective metallization to prevent oxidation of, and facilitate soldering to, the copper. Process variations investigated included outer layer composition (tin, tin-lead solder), application method (electrolytic, electroless) and "T" circuit delineation procedure.

The procedure initially involved successive vacuum depositions of nichrome and copper followed by an electrodeposition of tin-lead solder over the entire board. Riston was applied and the negative "T" pattern exposed and developed. Ferric chloride was used to remove the solder and copper layers exposed by the Riston mask. The length of time required for the etch treatment, however, resulted in severe undercutting and some loss of pattern resolution.

In a following revision, nichrome and copper again were deposited in succession. This time, however, preparation was made to limit the tin-lead deposit only to the "T" circuit. This required the use of a positive "T" pattern artwork which was used on the Riston layer applied to the copper layer. Exposure and development was followed by a tin-lead electroplate, after which the residual Riston was removed. The tin-lead plate then served as a mask for the following etches: chromic acid-sulfuric acid, to remove the copper; and ceric sulfate, to remove the nichrome. The thickness of the nichrome layer, however, necessitated an excessively long etch treatment which again resulted in some undercutting.

In another modification exactly the same procedure was followed but a thinner nichrome deposition was specified. The ceric sulfate etching again was too slow, either because the metallization was still too thick or because the Ni/Cr ratio was unfavorable. Proceeding on the latter assumption (Ni-rich) an HCl solution was substituted for the ceric sulfate with prompt results. However, the prolonged treatment again resulted in some damage, including solder-plate discoloration and partial removal at isolated points. Nevertheless, circuit definition on the whole (5-mil lines and 5-mil spacings) appeared to be clean and exact, a fact confirmed by microscopic examination.

The rather granular appearance of the solder-plated surfaces led to the consideration of pure tin as the final layer. This could be applied either by electroless or electrolytic means, both of which were investigated. In the electroless application the circuitry ("T" pattern) was masked with Riston prior to etch-removal of unwanted copper-nichrome. The filled vias, however, were not precisely planar with the adjoining circuit layer, which presented a problem of Riston adhesion at those locations. This, in turn, introduced some vulnerability to "lifting" during the following etching step. Subsequent removal of the Riston by normal solvent technique then resulted in some loss of z-direction conductor. The uncertain adhesion of Riston and potential etch undercutting at via sites were sufficient basis for discarding the electroless tin method.

In the electrolytic process Riston again was bonded to the copper-nichrome layer but in this case the T pattern was unmasked while all other areas remained protected. Electrical contact then was made to the copper layer for electrodeposition of tin exactly as was done in the solder-plate process described above. After "T" pattern deposition of the tin, the Riston was stripped off and the copper-nichrome layer thus exposed, etched away. Undercutting still remained a problem in cases of particularly etch-resistant nichrome, a problem that later was solved by a brief stannous chloride treatment (as discussed previously) prior to etching. The outer tin coating thus produced was finer-grained and more uniform than the previous solder-plates and it served its intended function in protecting the copper layers.

Gold-Polyimide Composite. — Early electrical tests indicated a higher incidence of anomalously high circuit impedance on boards with gold-filled z-direction conductors than on the purely organic-filled boards. This initially surprising observation was explained tentatively on the basis of the relative densities of the two fillers, both of which were bonded with polyimide varnish. Being 14 to 15 times as dense as the varnish medium, the gold would have a tendency to settle out if the maximum packing density of the particles had not been achieved on the initial application. Such settling, in turn, would encourage the formation of dielectric skin on top of the deposit, turning the excellent insulating properties of the polyimide into a liability. The organic conductor, even though a "pyrolyzate", was unlikely to have a density substantially greater than the bonding medium, itself, and would tend to retain its initial packing distribution.

It was found possible to "recover" many of the high impedance sites by cautious administration of voltage pulses but such recoveries were found to be only temporatily effective. The remedy adopted was to utilize as high a proportion of gold as possible (90 percent, or better) in the z-direction conductor formulation and to abrade away excess surface films where their presence was suspected on gold-filled vias.

Operator Dependence. — Throughout the fabrication phase of this program evidence accrued suggesting an interaction between process techniques as established and the conduct of these steps by the individual operator. The process consequences seemed to lie in long-term drift in control of sensitive procedures or in the sporadic appearance of recurring problems. The remedies employed were to advance, where possible, the operator's understanding of the applicable physical principles and to be watchful for signs of departure in established procedure.

It will be recognized, however, that an operator was obliged to become master of a great variety of process techniques and to coordinate them in such a way as to minimize the time and labor required to produce each finished article. Added to this was the evolving nature of the technology itself, which repeatedly required the judicious application of change to process techniques. In view of these considerations an operator dependence was just as much to be expected at this stage as it should be correctible at a later stage of development.

Fine-Line Displacement. – One effect that initially appeared to be operator dependent was the occasional displacement of 5-mil conductor lines which demanded extreme care in processing. Although not specified as a program requirement, retention of 5-mil geometry was thought to be well within the technology. The particular process step investigated for a solution to the problem was the 88 deg C baking of the Riston after lamination to the metallization layer. An increase in baking period would firm up the Riston and improve its mechanical strength against subsequent solvent treatments; a decrease would have the opposite effect but would facilitate subsequent stripping. The baking period, originally 10 min, was therefore increased to 18 min, producing fine-line geometry considerably less vulnerable to mechanical displacement and 100 percent yield. On the other hand, baking of the Riston on the copper metallizations (in preparation for via etching) was reduced to five minutes, or less, in order to facilitate subsequent stripping. This also proved successful, yielding a clean delineation of vias. (The hole geometry was well supported by the bulk of surrounding Riston and required only minimal cure to keep it in place; the opposite situation existed in fine-line retention). The results emphasized the interdependence of process steps and necessity for tailoring each step with full regard for the materials properties and geometries involved to achieve optimum process results.

Fabrication Log

Recorded in Table VI is a summary of monthly fabrication progress. Boards are identified by number in the left-hand column. Start of fabrication is indicated by month at the starting position of the line following board identification. Completion is indicated by a triangle. Seventy-five percent of the boards on aluminum, and 88 percent of those on Vespel, were dropped from further processing for the reasons identified by letter symbols. Many of these casualties led to improved processing techniques as discussed in the previous section. Others (designated by "F") suffered only minor flaws, such as off-center registration, edge damage (curling), minor nichrome residues, etc., many of which would have been recoverable by further processing. Lines which terminate without a triangle, or other symbol, represent boards carried satisfactorily to a particular point in processing from which their continued fabrication could be resumed if later required.

In Table VII the final disposition of boards is summarized. The format of this table was used in periodic reporting of progress in fabrication as defined by the major processing steps. Boards 19, 20, 21, 31, 34, 35, 36 and 37 on aluminum, and boards 11 and 14 on Vespel, were completed. Boards 1 and 4 on aluminum also were carried to completion, but with the z-direction conductor omitted because composite compositions and application methods still were under development. Of the completed boards, Numbers 31, 35 and 36 on aluminum, and 11 and 14 on Vespel were subjected to environmental stress cycling, as described in the following section. Not included in Table VII are boards dropped from further processing.

TABLE VI
BOARD FABRICATION LOG

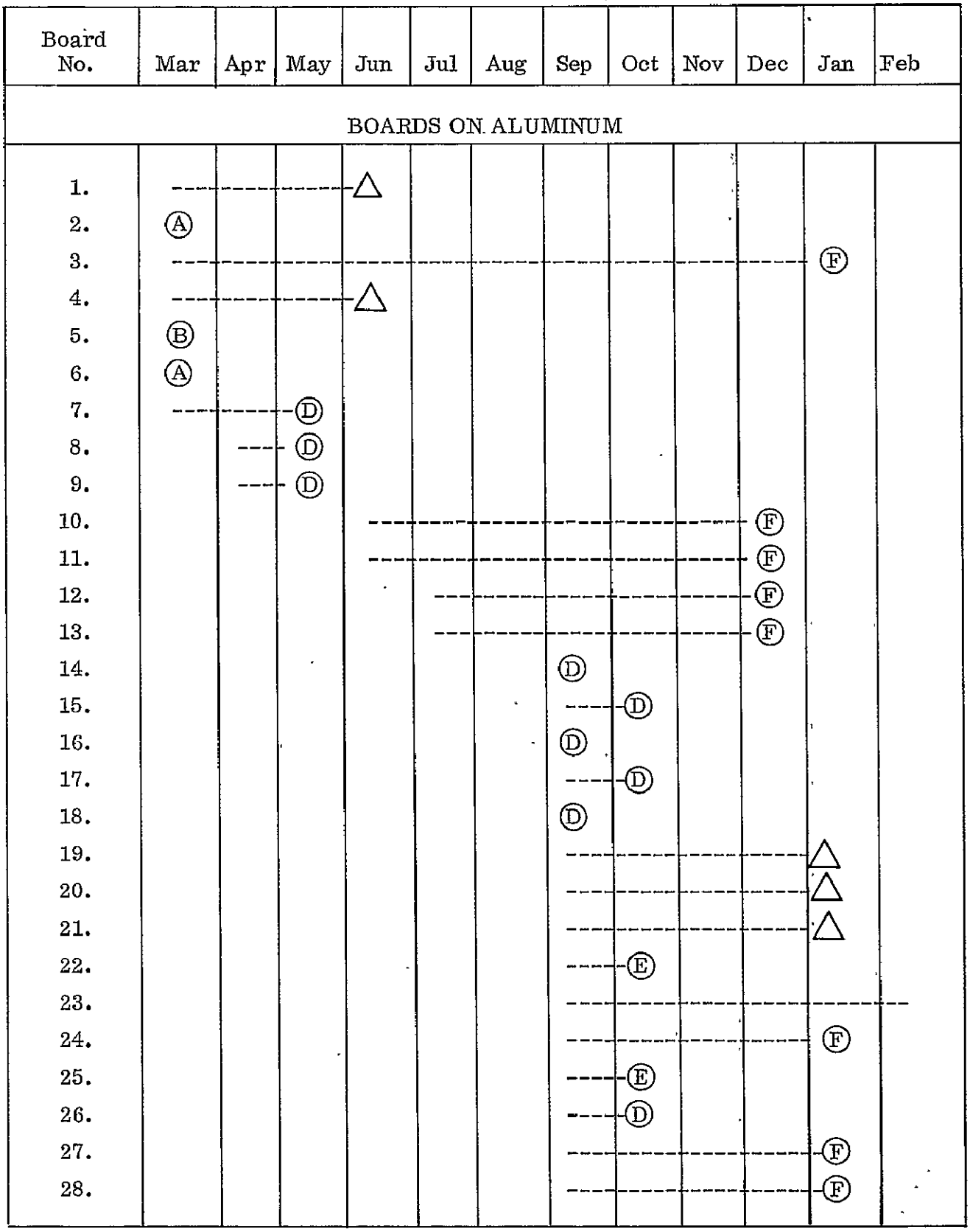


TABLE VI
BOARD FABRICATION LOG (Cont)

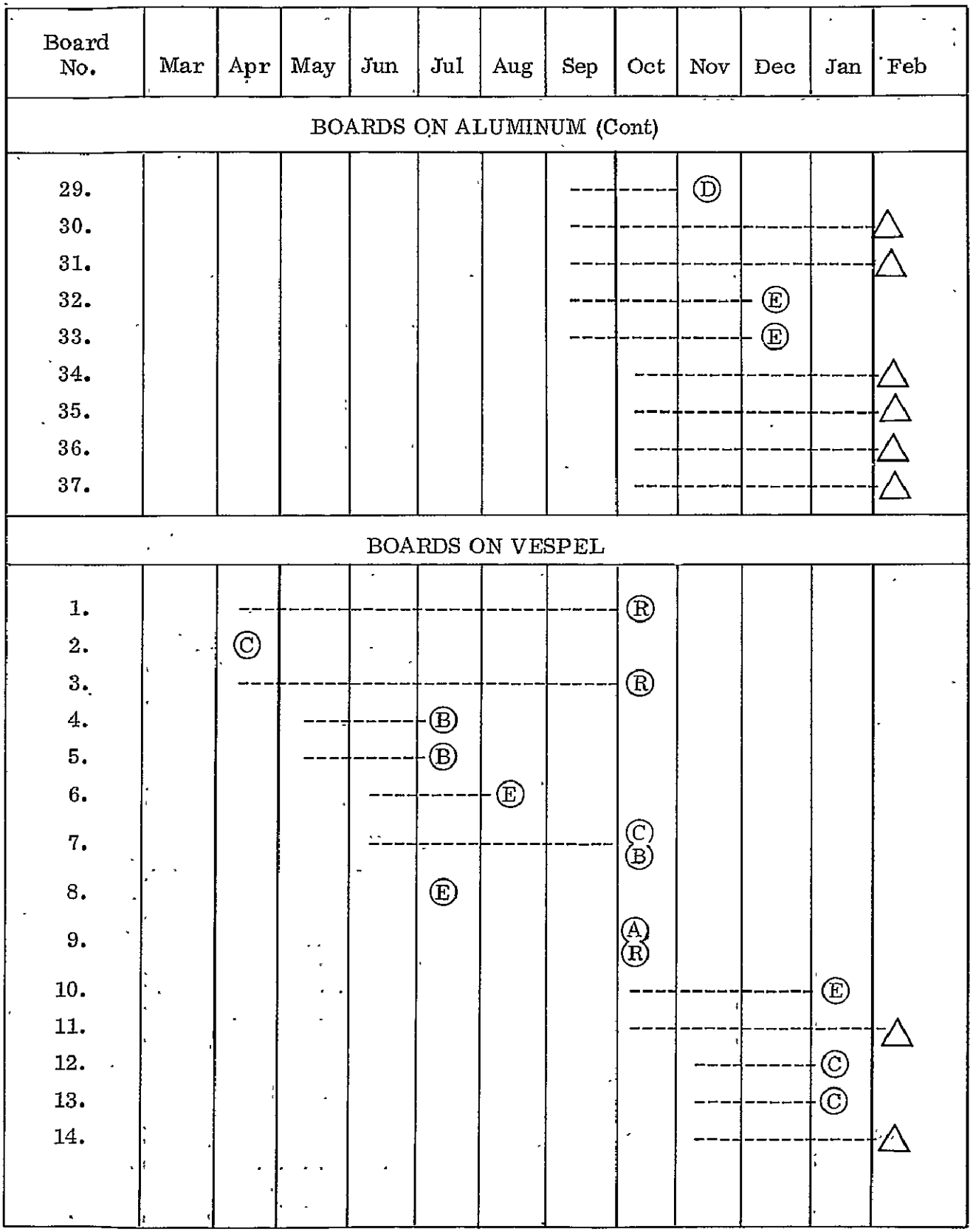


TABLE VI
BOARD FABRICATION LOG (Cont)

Board No.	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb
BOARDS ON VESPEL (Cont)												
15.									----	----	----	----
16.									----	----	----	----
17.									----	----	----	----

Legend:

A: Riston Adhesion
B: Over-cure
C: Warping
D: Diverted to Experiments
E: Blistering
F: Minor Defects, often reparable
△: Completion
R: Recycled following appearance of minor imperfections

BOARD TESTING

Preliminary Test Results

In fulfilling the requirements of Item 6 of the Statement of Work, which calls for exposing finished circuit boards to an environmental stress regime, it was considered advisable to establish the pertinent boundary conditions well in advance of when they would be needed. This action was taken on a limited scale at a time when the leading boards were only half way through processing (at Step 10). The tests were confined to three boards on aluminum (No.'s 15, 17 and 26), each having only one buried circuit layer. They were "completed" by inoculation with organic 3-direction conductor, followed by deposition and delineation of a copper/tinplate "T" pattern (Steps 17-20). In addition to fixing exposure limits the tests could be expected to give advance indication of any hitherto unobvious incompatibilities in materials or treatments.

TABLE VII
FABRICATION PROGRESS CHART*

Substrate	Al	Al	Vespel
1. Polyimide base layer			
2. Circuit layer No. 5			
3. Polyimide, b-stage		3	
4. Cu mask B-1, etch		11, 12, 13	
5. Fill thru-holes	omit	10	omit
6. Circuit layer No. 4			
7. Polyimide, b-stage			
8. Cu mask B-2, etch			
9. Fill thru-holes	omit	omit	omit
10. Circuit layer No. 3		32, 33	
11. Polyimide, b-stage			
12. Cu mask B-3, etch			17
13. Fill thru-holes	omit	omit	omit
14. Circuit layer No. 2		24, 27	15, 16
15. Polyimide, b-stage			
16. Cu mask B-4, etch	23	28	
17. Fill thru-holes			
18. NiCr/Cu Deposit			
19. Tin-plate, "T" pattern			
20. Final etch			

*Completed: Numbers 19, 20, 21, 30, 31, 34, 35, 36 and 37 on Al;
Numbers 11 and 14 on Vespel.

Thermally Cycled: Numbers 31, 35 and 36 on Al; Numbers 11 and 14 on Vespel.

After initial electrical measurements the boards were carried through eight thermal cycles from -65 to +125 deg C. The single-cycle period was 2.67 hours. The effects of this cycling on circuit* resistance are given in Table VIII.

TABLE VIII
EFFECT OF THERMAL CYCLING ON CIRCUIT RESISTANCE

Resistance (Ohms)		$\triangle$R	Line Width
Before Cycling	After Cycling	(Percent)	(Mils)
0.83	0.82	-1.2	40
1.01	1.00	-1.0	40
2.04	2.01	-1.5	20
4.03	4.60	+14.2	10
4.37	4.56	+4.4	10

All circuits were of identical length with line widths as specified in the table. Casual inspection of the results indicates a resistance dependence on line width, placing the main component of resistance in the lines themselves. Indeed, a plot of reciprocal resistance against line width produces a straight line through the origin, suggesting a negligible contribution from the z-direction conductors. The highly favorable cross-section-to-length ratio of the vias, no doubt, is a contributing factor. On the basis of this limited evidence, however, it could not be assumed that via resistance contributions would be insignificant in all cases.

The effect of the thermal cycling on resistance measurements was negligible except for the two 10-mil lines. This suggested a possible limiting value for line width; the five-mil lines in this specimen were inoperative both before and after the cycling. Determining the exact cause of the resistance changes would have required a detailed failure analysis.

*"Circuit", as employed herein, refers generally to a simple board element consisting of a buried conductor line, including (where applicable) its z-direction conductor and "T" layer metallization termini. It also may consist of an external resistor soldered to a pair of "T" layer pads and contiguous conductors, or to probe sites used in testing for dielectric current leakage.

In a further test a two-inch length of 25-mil gold plated copper wire and an integrated circuit were soldered to pads on the "T" circuit layer. No unusual problems were encountered in the soldering process. Adhesion strength of the solder bond was remarkably strong, being in excess of one pound pull strength in the case of the single wire. Visual examination revealed no evidence of material degradation in or near the bonding sites.

Another specimen, instead of receiving an electroplate of solder (Step 19), was float-soldered directly at a temperature of 257 deg C. The treatment resulted in extensive parting of the circuit layers from the substrate. The specimen had received no desiccation or heating to outgas moisture (which can be as high as two percent by weight of the polyimide) prior to the treatment. Appropriate thermal or outgassing pretreatments should make this method a practical alternative to electroplating.

In view of the preliminary results described above it was decided that the finished boards could be made to yield useful information by undergoing a prolonged series of thermal cycles, both at average humidity (50 to 60 percent relative) and at high humidity (90 percent relative), but that a thermal shock treatment would have consequences drastic enough to render the boards unsuited for many subsequent tests. Therefore final board testing was confined to an analysis of the effects of thermal cycling only, as described in the following section.

Environmental Testing

Specimen Preparation. – Environmental thermal cycling was initiated on five boards as soon as they were completed: Boards 31, 35 and 36 on aluminum, and Boards 11 and 14 on Vespel. Boards 14, 31 and 36 had organic z-direction conductors; the remainder utilized gold-filled polyimide as the z-direction conductor material. The group therefore contained all four combinations of z-direction conductor and substrate materials due for delivery under the terms (Item 3) of the contract.

Electrical resistances were measured on all circuits prior to inoculation with z-direction conductor in order to ensure the detection of any significant changes introduced by application of these materials. These data, labeled "B. F." and "A. F." ("before filling" and "after filling"), are conveniently combined with all subsequent resistance measurements in a single set of tables later in this section.

In continued fulfillment of the requirement to demonstrate solderability of components to the boards (Item 5) four ten-ohm resistors were soldered to each of the boards prior to cycling. Some difficulty in soldering was encountered due to an

apparent excessive thinness* of the copper layers (and probably to the presence of sufficient tin-plate) which resulted in copper depletion. The problem was particularly acute where poor heat transfer conditions prevailed, i.e., on the Vespel boards, and very short iron dwell times were required. Attachment of resistors to board 14 on Vespel was only 50 percent effective (in the sense that only two of the four resistors were attached as initially planned), and further casualties were to be anticipated on prolonged thermal cycling. The problem was not observed in the prior soldering experiments where only aluminum substrates were tested and the copper layer was solder-plated rather than tin-plated. The observed soldering difficulty on the Vespel boards, however, should not be taken as an inherent flaw in the compatibility of the materials employed but as an indication that the procedures utilizing these materials require further optimization. Remedial modifications, such as thickening the copper deposit and/or preheating the Vespel boards prior to soldering, can be utilized if continued development appears justified.

Test Schedule. — Environmental cycling was conducted over a two-month interval toward the end of the contract period. The five boards identified above were exposed to 427 cycles having a three-hour periodicity and a repeating temperature excursion of -55 to +100 deg C**. The first 216 cycles were conducted at ambient humidity (40 to 65 percent relative) and the last 211 cycles at 90 percent RH. Electrical measurements were made on the boards at 0, 30, 52, 106, 216, 234, 263, 317 and 427 cycles. The measurements included resistance determinations on 58 circuits per board and 17 dielectric leakage tests per board, yielding approximately 3300 datum points that reflected the effects of the environmental cycling on electrical performance.

Selection of Test Sites. — All electrical measurements are identified and coded in Figure 16, which displays the top circuit pattern in solid colors and underlying circuits as dashed lines. There are four circuit levels below the "T" layer, designated as 5, 4, 3 and 2 on the artwork, with Layer 5 next to (but electrically isolated from) the substrate, and Layer 2 next to the "T" layer. Circuits of similar configuration are grouped together under a single letter symbol. Group A1 to A4, for example, consists of 40-mil lines with A1 at Layer 2 and A4 at (the bottom) Layer 5. Set B is similarly organized but consists of 20-mil lines. Sets C and D have 10- and 5-mil lines respectively.

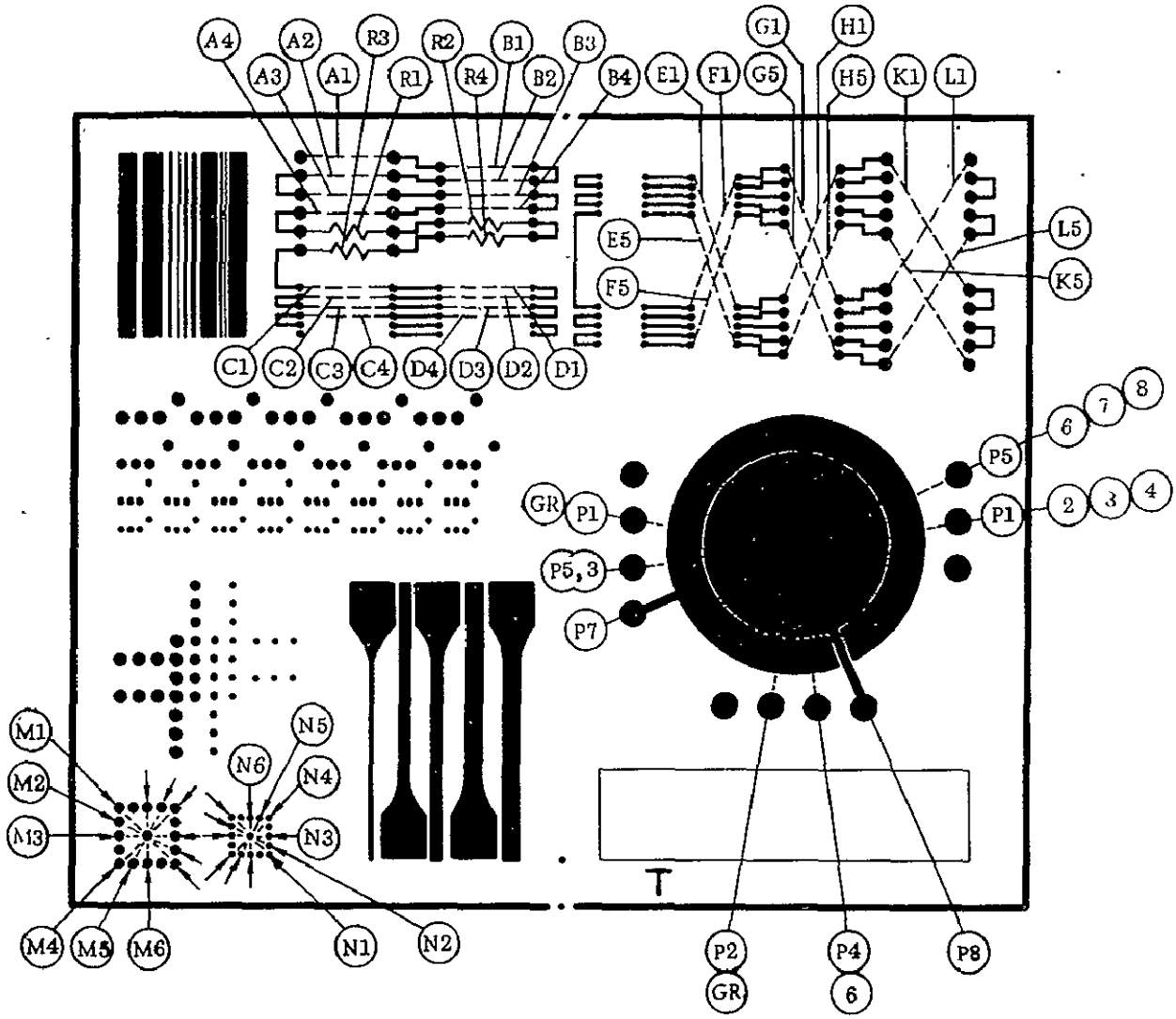
Resistors R1 to R4 are soldered to the indicated pads on the "T" layer and lie on the board surface. These pads are otherwise isolated from each other because underlying circuits have been left out.

In Sets E through L the intervening Circuits 2, 3 and 4 have been deliberately omitted to preserve clarity. For the same reason these circuits have been represented by diagonals rather than attempting to delineate their actual square "S" contours (see Figure 9), which overlie each other at adjacent circuit levels. Group E1 to E5 lies entirely at Level 5; group F1 to F5 lies at Level 4 and overlays set E. Sets G and K lie at Level 3; Sets H and L, at Level 2. Sets E and F consist of 10-mil lines; Sets G and H, 20-mil lines; Sets K and L, 40-mil lines.

In Sets M and N probe contacts are represented by arrows situated at opposite ends of each line and designate the circuit measurement identified by the assigned

*Approximately 20,000 Å.

**Rise time: 90 min.; fall time: 75 min.; soak time (high): 10 min.; soak time (low): 5 min.



Legend:

All underlying circuits are represented by dashed lines.

All electric probe measurements are identified by group and number, and include resistances of the terminal vias where applicable.

Ten ohm (1 percent) resistors R1 to R4 are soldered to the indicated surface pads where underlying shunt lines have been omitted.

Although not explicitly represented in the diagram, E2, E3 and E4 are situated sequentially between E1 and F5. The same applies to Groups F, G, H, K and L. Circuits in these groups actually are square "S"-shaped but for further clarity are depicted as diagonals.

Capacitor leakage measurements are identified by the terminals probed, e.g., P1-1, P2-2, etc. Electrical leakage measurements to the substrate apply to boards on aluminum only and are identified as GR1 and GR2. Consult accompanying text for further details.

Figure 16. Top Circuit Layer (Probe Test Designations)

symbol. In both sets, Lines 1 and 4 lie at Level 2; Lines 2 and 5, at Level 3; Lines 3 and 6, at Level 5. Lines at Level 4 are absent in both sets.

Capacitor measurements are designated by P. The top capacitor plate consists of two electrically isolated and independently terminated metallizations, one being a central circular area with Terminus P8, the other, an outer annulus with Terminus P7. Directly beneath this pair, and isolated from it by a polyimide layer, lies a single circular metallization (Level 2) whose outer contour coincides with that of the top annulus, P7, and which terminates at the pad identified as P5 (6, 7, 8). The additional numbers appended to this terminus serve to identify the various dielectric leakage measurements requiring the use of this capacitor plate. Thus, the designation P8-8 is the measurement between Termini P8 and P5 (6, 7, 8), or between the top central capacitor plate and the Layer 2 capacitor plate directly below it. Similarly, the designation P7-7 applies to P7 and P5 (6, 7, 8), or the measurement between the top annular plate and the same underlying plate.

There are a total of three dual-plate combinations, each consisting of a central circular plate and a coplanar annulus, identified as P7 – P8; P5, 3 – P4, 6 and P1, GR–P2, GR. They are situated respectively at Levels "T", 3 and 5. The intervening solid circular plates are P5 (6, 7, 8) at Level 2 and P1 (2, 3, 4) at Level 4. All of the plates are electrically isolated from each other, and from the substrate, by the thin (200 to 250 microinch) polyimide films.

The dual combinations are separated by a lateral spacing of 10 mils and afford a means of testing for current leakage between adjacent conductors on the same circuit level. These tests are identified in the following tables according to the dual-plate designations given above but abbreviated to: (GR)P1-2 (at Level 5); P5, 3 – 4, 6 (at Level 3) and P7-8 (at Level "T").

Leakage to ground pertains only to the aluminum substrates and is measured from the lowermost dual combination to the metal base. The tests are identified as GR1 and GR2 in the tables.

Capacitor measurements other than current leakage tests were considered but could not be scheduled in the time available.

Procedure and Evaluation Criteria. – Electrical tests were designed to serve three purposes: to monitor fabrication techniques; to demonstrate functionality of completed boards; and to reveal performance trends during environmental cycling. In view of the desirability of generating a statistically significant number of data, and of the substantial number of test sites to be monitored therefor, electrical probing by hand with a VOM was considered the only practical procedure. Although some error in measurements can be anticipated as a result of small contact areas, variations in contact pressures and occasional intervention of electrically resistive films, the magnitude of such errors was not expected to be great enough, in most cases, to occlude important trends in performance induced as a result of fabrication technique or thermal cycling.

Measurements were designed to determine both conductor performance and dielectric performance. In both cases performance was evaluated in terms of electrical resistance and recorded in ohms. The range of measurements was determined by

the instrumental capability which, in this case, lay from approximately 0.2 ohms to 5×10^7 ohms. This automatically established the dielectric performance criterion at 5×10^7 ohms, since any observable meter deflection was accepted as a failure. This was known to be a somewhat generous performance limit for the polyimide because the reported volume resistivity (Ref 8, p 115) is 10^{17} ohm cm which, in application to the present geometry, yields a minimum resistance of 10^{11} ohms between any two capacitor plates. According to the available evidence, however, the detection of dielectric defects was unequivocal because their "resistance values" all lay below four ohms. This does not remove the possibility of current leakage effects represented by the excluded region above 5×10^7 ohms but it does clearly identify the more serious type of defect. The same standard was adopted in the detection of lateral (line spacing) current leakage between conductors and, in the case of aluminum substrates, leakage to ground.

Performance criteria for conductor paths were less readily defined because of the lack of an established prior art, the absence of a minimum acceptable conductivity based on end-use requirements and the as yet imperfectly understood effects of several of the process variables alluded to earlier in this report. It was particularly difficult to decide upon qualification limits in base-line resistance values, i.e., those values measured prior to environmental cycling. Many abnormally high beginning resistance values displayed remarkable internal consistency, either as a group or sequentially, which bespoke an inherent stability and materials compatibility in the presence of a temporary drift in some process parameter. Such data could not be arbitrarily rejected without sacrifice of numerical weight applicable to the analysis of performance trends. Consequently all data were retained and no acceptance limits placed on base-line values.

The observation of performance trends during the course of environmental cycling proved more meaningful but again necessitated the establishment of an artificial boundary limit upon which these trends could be judged. In this case an arbitrary selection rule would not necessarily undermine the approach to meaningful conclusions. The rule adopted defined failure as an increase in observed circuit resistance to a value at least twice that of the base-line value. A failure distribution based on this formula permitted tentative inferences to be drawn in the absence of a more formal, and possibly less conservative, definition based on actual performance requirements.

Organization of Data. – Electrical performance data before, during and after environmental cycling are listed in Tables IX, X, XI, XII and XIII. The circuit board represented by each table is identified at the top by its number, substrate material and z-direction conductor material. The circuits measured are identified in the left-hand column according to the test site designations indicated in Figure 16. Columns "BF" and "AF" list measurements made before and after filling of the vias with z-direction conductor. Numerical entries are in ohms. Entries of "NR" stand for no detectable reading. In these cases the impedance exceeds 5×10^7 ohms and the circuit is presumed open. Entries of "OK" apply to tests of dielectric integrity and indicate no detectable current leakage or failure; impedance exceeds 5×10^7 ohms. Dashes indicate omission of measurements for any of several reasons, such as total loss of a component or a section of conductor, lack of meaningfulness (e.g., resistor sites prior to soldering; leakage to ground on Vespel boards) and measurements not included in the initial test plan. Other entries are self-explanatory.

TABLE IX
EFFECT OF ENVIRONMENTAL CYCLING ON CIRCUIT PERFORMANCE
Board: 31 Substrate: Aluminum Vias: Organic

Circuit	Resistance (ohms)									
			Cycles Completed, -55 to +100°C				Ditto, but at 90% R.H.			
	B.F.*	A.F.*	30	52	106	216	234	263	317	427
A1	--	0.5	0.7	0.5	0.5	0.6	0.5	0.6	0.6	0.7
2	--	1.4	1.6	1.5	1.4	1.5	1.5	1.6	1.6	1.7
3	--	0.7	0.8	0.7	0.6	0.8	0.7	0.8	0.8	0.9
4	--	1.1	1.4	1.1	1.1	1.2	1.2	1.4	1.3	1.4
B1	--	0.7	0.9	0.7	0.7	0.8	0.9	0.9	0.9	1.0
2	--	2.0	2.4	2.2	2.1	2.3	2.4	2.5	2.5	2.9
3	--	0.9	1.1	1.0	0.9	1.0	1.1	1.1	1.1	1.3
4	--	1.5	1.8	1.8	1.5	1.8	1.9	1.9	1.9	2.1
C1	1.0	1.3	1.4	1.2	1.2	1.3	1.3	1.3	1.3	1.5
2	4.0	1.4	1.6	1.5	1.4	1.6	3.5	4.3	4.3	4.5
3	1.4	1.2	1.5	1.4	1.5	1.5	2.5	3.3	3.5	4.3
4	2.4	2.3	2.6	2.5	2.5	2.6	2.7	2.7	2.7	3.2
D1	2.6	2.2	2.4	2.2	2.4	2.4	2.4	2.4	2.4	2.5
2	9.5	2.4	2.6	2.5	2.7	2.6	2.7	2.7	2.8	2.9
3	7.4	5.0	5.3	5.3	5.4	5.5	5.8	5.9	6.2	8.2
4	7.4	5.5	6.1	6.1	6.2	6.3	7.0	7.5	8.5	14.5
E1	7.5	3.4	4.9	4.7	4.7	5.0	5.9	7.1	7.3	7.5
2	6.5	3.4	5.0	4.8	4.7	5.0	6.0	7.2	7.5	10.8
3	6.5	6.7	7.2	7.2	6.8	7.4	7.5	7.4	7.4	7.6
4	6.3	6.3	6.9	6.8	6.6	7.4	7.8	15.5	16.0	18.0
5	6.3	6.3	10.6	10.7	10.7	11.2	12.5	13.5	14.0	15.0
F1	3.6	3.6	4.0	3.8	3.6	3.7	3.9	4.0	5.4	4.2
2	4.2	3.6	3.9	3.8	3.7	3.7	3.9	4.0	5.4	4.3
3	3.6	3.7	3.9	3.9	3.7	3.7	3.9	4.0	5.4	4.3
4	3.5	2.6	3.7	3.6	3.5	3.6	4.1	4.6	5.1	5.3
5	3.6	2.6	3.7	3.7	3.6	3.7	4.1	4.2	5.1	4.7
G1	5.2	4.9	5.2	5.2	5.1	5.1	5.2	5.3	5.3	5.5
2	5.2	3.3	5.1	5.2	5.1	5.3	5.2	5.4	5.3	5.6
3	5.3	3.2	5.0	5.1	5.0	5.3	5.2	5.3	5.3	5.6
4	5.3	4.3	6.4	6.6	6.5	6.8	5.8	6.1	6.1	6.6
5	5.6	3.9	5.0	5.2	5.2	5.2	5.1	5.1	5.1	5.3
H1	2.0	1.3	1.4	1.5	1.5	1.5	1.6	1.7	1.8	1.9
2	2.0	1.3	1.4	1.6	1.5	1.5	1.6	1.7	1.8	1.9
3	2.2	1.6	1.5	1.7	1.7	1.7	1.8	1.8	1.8	2.0
4	1.9	1.8	1.9	1.9	1.7	1.8	1.8	2.0	2.2	2.4
5	2.1	1.7	1.9	1.8	1.8	1.8	1.9	1.9	1.9	2.1
K1	5.0	2.6	3.2	3.2	3.1	3.1	3.3	3.5	3.5	3.8
2	4.8	2.5	2.9	2.8	2.7	2.8	2.9	3.2	3.1	3.3
3	5.5	4.3	4.7	4.7	4.7	4.8	4.8	4.9	4.9	5.1
4	5.0	4.1	4.4	4.3	4.3	4.5	4.4	4.6	4.6	4.8
5	5.3	4.1	4.4	4.2	4.2	4.3	4.3	4.4	4.4	4.8

TABLE IX
EFFECT OF ENVIRONMENTAL CYCLING ON CIRCUIT PERFORMANCE (Cont)
Board: 31 Substrate: Aluminum Vias: Organic

Circuit	Resistance (ohms)									
			Cycles Completed, -55 to +100°C				Ditto, but at 90% R.H.			
	B.F.*	A.F.*	30	52	106	216	234	263	317	427
L1	1.8	1.4	1.6	1.4	1.4	1.4	1.4	1.5	1.5	1.7
2	2.0	1.4	1.8	1.8	1.8	1.7	1.8	2.0	2.0	2.3
3	1.7	1.3	1.7	1.5	1.6	1.5	1.5	1.6	1.7	1.8
4	2.2	1.3	1.6	1.4	1.5	1.4	1.5	1.5	1.5	1.7
5	2.2	1.4	1.6	1.5	1.6	1.5	1.6	1.6	1.5	1.8
M1	0.7	0.5	0.9	0.6	0.7	0.6	0.6	0.7	0.7	0.8
2	1.9	1.7	1.9	1.9	1.9	1.9	1.9	1.9	2.0	2.1
3	0.8	1.0	1.5	1.5	1.5	1.5	1.8	1.9	2.1	2.4
4	0.6	0.5	0.8	0.7	0.7	0.6	0.6	0.7	0.7	0.8
5	1.8	1.6	1.8	1.8	1.8	1.7	1.8	1.9	1.9	2.0
6	2.0	0.9	1.1	1.1	1.1	1.1	1.3	1.4	1.5	1.7
N1	0.7	1.0	0.8	0.8	0.8	0.7	0.8	0.8	0.8	1.0
2	1.8	1.8	1.8	1.9	1.9	1.9	1.9	1.9	2.0	2.2
3	N.R.	1.1	1.2	1.4	1.4	1.3	1.9	7.8	7.9	8.4
4	0.7	0.7	0.7	0.8	0.8	0.7	0.7	0.8	0.8	1.0
5	1.8	2.2	4.1	4.7	4.6	4.2	4.8	4.4	4.4	4.4
6	1.2	0.8	0.8	1.0	1.0	0.9	1.3	1.4	1.5	1.6
P1-1	OK***	OK	OK	OK	OK	OK	OK	OK	OK	OK
2-2	short	1.5	1.8	1.5	1.4	1.4	1.3	1.4	1.5	1.6
3-3	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
4-4	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
5-5	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
6-6	short	1.7	2.1	1.9	1.9	1.9	1.9	1.9	1.9	2.1
7-7	--	--	OK	OK	OK	OK	OK	OK	OK	OK
8-8	--	--	OK	OK	OK	OK	OK	OK	OK	OK
GR1	--	OK	OK	OK	OK	OK	OK	OK	OK	OK
2	--	OK	OK	OK	OK	OK	OK	OK	OK	OK
(GR)P1-2	--	OK	OK	OK	OK	OK	OK	OK	OK	OK
P5,3-4,6	--	OK	OK	OK	OK	OK	OK	OK	OK	OK
P7-8	--	--	1.0	0.7	0.7	0.8	0.7	0.9	0.9	1.1
R1	--	--	10.7	10.5	10.1	10.5	10.2	10.6	10.8	10.9
2	--	--	10.9	10.5	10.2	10.5	10.4	10.7	10.8	10.9
3	--	--	10.9	10.5	10.1	10.4	10.3	10.7	10.8	10.9
4	--	--	10.9	10.4	10.1	10.4	10.3	10.6	10.8	10.9

*B.F.: Before filling of vias; A.F.: After filling of vias, but before commencement of environmental cycling.

***No detectable current leakage or dielectric failure.

TABLE X
EFFECT OF ENVIRONMENTAL CYCLING ON CIRCUIT PERFORMANCE
Board: 36 Substrate: Aluminum Vias: Organic

Circuit	Resistance (ohms)									
			Cycles Completed, -55 to +100°C				Ditto, but at 90% R.H.			
	B.F.*	A.F.*	30	52	106	216	234	263	317	427
A1	0.6	0.6	1.3	0.8	0.9	0.8	0.8	0.7	0.8	0.9
2	1.0	1.0	1.6	1.3	1.3	1.3	1.2	1.2	1.3	1.3
3	11.0	10.0	10.5	11.0	10.9	11.0	11.0	11.0	11.0	11.4
4	0.5	0.9	1.2	1.1	1.2	1.3	2.1	2.6	3.3	4.2
B1	0.8	0.9	1.3	1.1	1.2	1.3	1.2	1.0	1.1	1.2
2	1.5	4.5	5.0	4.8	4.9	5.2	5.5	9.0	10.5	15.0
3	15.0	15.0	16.0	16.5	16.5	17.0	18.0	51.0	57.0	63.0
4	0.7	1.0	1.6	1.5	1.5	1.8	3.9	1.8	8.5	4.7
C1	1.8	1.8	2.3	2.2	2.2	2.2	2.2	2.1	2.2	2.3
2	2.6	2.6	2.8	3.1	3.1	3.1	3.1	3.0	3.1	3.2
3	27.0	25.0	28.0	28.0	28.0	27.0	29.0	28.0	28.0	30.0
4	1.7	1.8	2.0	2.2	2.2	2.2	2.3	2.1	2.2	3.1
D1	3.4	3.5	3.8	4.2	4.1	4.1	4.3	4.1	4.2	4.4
2	6.0	6.2	6.6	7.0	6.8	7.0	7.2	7.0	7.0	7.2
3	66.0	70.0	68.0	68.0	68.0	68.0	71.0	69.0	70.0	70.0
4	4.0	5.5	5.7	5.8	5.9	6.5	10.0	12.0	14.0	16.0
E1	2.8	5.6	5.1	5.3	5.3	5.4	9.2	11.0	12.5	15.0
2	2.8	4.2	4.3	4.5	4.5	4.8	11.0	15.0	19.0	25.0
3	2.8	5.0	5.3	5.0	5.0	5.2	8.2	9.8	11.5	14.0
4	3.1	3.2	3.9	3.6	3.6	3.5	3.8	4.0	4.2	130.0
5	--	4.6	5.2	5.1	5.2	5.6	9.5	11.2	13.0	15.0
F1	67.0	73.0	72.0	72.0	72.0	72.0	77.0	128.0	145.0	162.0
2	66.0	80.0	80.0	81.0	81.0	81.0	94.0	109.0	125.0	159.0
3	66.0	70.0	68.0	69.0	68.0	68.0	71.0	69.0	70.0	70.0
4	66.0	N.R.**	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.
5	66.0	78.0	76.0	76.0	77.0	76.0	90.0	100.0	109.0	115.0
G1	4.0	3.7	4.6	4.4	4.3	4.3	4.4	4.3	4.4	4.3
2	4.0	3.8	4.7	4.5	4.4	4.4	4.5	4.4	4.4	4.4
3	4.0	3.8	4.6	4.5	4.5	4.5	4.5	4.4	4.5	4.4
4	4.1	3.9	4.7	4.5	4.5	4.5	4.6	4.4	4.5	4.4
5	4.0	3.8	4.5	4.5	4.3	4.3	4.5	4.2	4.4	4.4
H1	1.8	1.4	2.3	2.2	2.1	2.0	2.1	2.0	2.1	2.0
2	1.8	1.4	2.4	2.2	2.1	2.0	2.1	2.0	2.1	2.0
3	1.8	1.7	2.3	2.2	2.2	1.9	2.0	1.9	2.0	1.9
4	1.8	1.7	2.4	2.2	2.2	2.0	2.1	2.0	2.1	2.0
5	1.8	1.8	2.3	2.2	2.2	2.0	2.1	2.0	2.0	2.0
K1	4.4	2.3	3.4	4.2	3.9	3.9	4.3	4.0	4.0	4.0
2	3.5	2.3	3.5	4.1	3.8	3.8	4.1	3.8	3.9	3.9
3	3.5	3.3	3.5	3.9	3.7	3.8	4.1	3.8	3.8	3.8
4	3.5	3.4	3.5	4.0	3.8	3.9	4.1	3.9	3.9	3.9
5	3.5	3.1	3.3	3.8	3.6	3.7	4.0	3.6	3.6	3.6

TABLE X (Cont)
EFFECT OF ENVIRONMENTAL CYCLING ON CIRCUIT PERFORMANCE (Cont)
Board: 36 Substrate: Aluminum Vias: Organic

Circuit	Resistance (ohms)									
			Cycles Completed, -55 to +100°C				Ditto, but at 90% R.H.			
	B.F.*	A.F.*	30	52	106	216	234	263	317	427
L1	1.4	2.3	1.5	1.5	1.6	1.6	1.9	1.6	1.6	1.6
2	1.5	2.3	1.6	1.6	1.7	1.6	1.9	1.6	1.7	1.7
3	1.5	3.4	1.6	1.6	1.8	1.7	1.8	1.6	1.7	1.6
4	1.5	3.5	1.5	1.6	1.7	1.7	1.8	1.6	1.7	1.6
5	1.5	3.3	1.6	1.6	1.7	1.7	1.8	1.6	1.7	1.7
M1	1.5	1.3	1.8	1.9	1.9	1.8	1.8	1.6	1.7	1.8
2	1.2	0.9	1.5	1.4	1.4	1.3	1.3	1.2	1.3	1.3
3	0.9	0.6	1.1	1.0	1.0	1.0	0.9	0.8	1.0	1.0
4	1.4	1.3	1.9	1.7	1.7	1.4	1.8	1.5	1.5	1.6
5	1.2	1.0	1.6	1.3	1.3	1.1	1.3	1.2	1.2	1.2
6	1.0	0.6	1.0	0.9	0.9	0.8	0.9	0.7	0.8	0.8
N1	1.3	13.0	22.0	30.0	27.0	37.0	60.0	13.0	25.0	18.0
2	1.4	5.0	5.2	5.7	5.8	6.4	9.4	10.5	14.0	14.0
3	4.0	1.1	1.6	1.5	1.5	1.4	1.8	5.5	23.0	4.0
4	1.3	1.2	1.3	1.4	1.4	1.3	2.0	1.3	1.4	1.4
5	1.3	1.2	1.4	1.5	1.5	1.4	1.8	1.4	1.4	1.5
6	N.R.**	N.R.	N.R.	6,400	6,200	6,400	12,000	N.R.	N.R.	N.R.
P1-1	OK***	OK	OK	OK	OK	OK	OK	OK	OK	OK
2-2	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
3-3	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
4-4	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
5-5	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
6-6	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
7-7	--	OK	OK	OK	OK	OK	OK	OK	OK	OK
8-8	--	0.3	0.9	0.6	0.6	0.8	0.8	0.6	0.6	0.6
GR1	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
2	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
(GR)P1-2	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
P5-3,4,6	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
P7-8	--	OK	OK	OK	OK	OK	OK	OK	OK	OK
R1	--	--	10.0	10.2	10.2	10.1	10.4	10.2	10.2	10.2
2	--	--	10.0	10.2	10.3	10.1	10.4	10.2	10.4	10.2
3	--	--	10.0	10.2	10.2	10.2	10.4	10.2	10.3	10.2
4	--	--	10.0	10.2	10.2	10.2	10.4	10.2	10.4	10.2

*B.F.: Before filling of vias; A.F.: After filling of vias, but before commencement of environmental cycling.

**No detectable reading. Impedance exceeds 5×10^7 ohms and circuit is presumed open.

***No detectable current leakage or dielectric failure.

TABLE XI
EFFECT OF ENVIRONMENTAL CYCLING ON CIRCUIT PERFORMANCE
Board: 35 Substrate: Aluminum Vias: Gold Filled

Circuit	Resistance (ohms)									
			Cycles Completed, -55 to +100°C				Dittó, but at 90% R.H.			
	B.F.*	A.F.*	30	52	106	216	234	263	317	427
A1	0.5	2.0	1.0	0.9	0.9	0.7	0.7	0.8	0.8	0.9
2	1.0	2.4	1.4	1.5	1.5	1.2	1.3	1.3	1.3	1.4
3	8.5	10.0	9.5	9.3	9.6	9.6	10.0	10.2	10.2	10.2
4	0.6	1.6	1.0	1.5	1.0	0.9	0.9	0.9	0.9	1.0
B1	0.8	1.8	1.1	0.9	0.8	1.0	1.0	1.0	1.0	1.1
2	1.6	2.6	2.0	2.0	1.9	2.0	2.0	2.1	2.1	2.1
3	12.5	25.0	23.0	24.0	24.0	25.0	25.0	23.0	28.0	19.0
4	1.0	1.2	1.3	1.2	1.1	1.2	1.3	1.3	1.3	1.4
C1	1.7	2.0	2.1	1.9	1.9	2.0	2.0	2.0	2.0	2.1
2	3.0	8.0	7.2	6.8	7.7	19.0	7.5	6.3	6.5	120.0
3	21.0	300.0	1,500	1,750	1,850	2,100	1,600	2,100	4,400	4,500
4	2.0	2.4	2.6	2.4	2.3	2.3	2.4	2.5	2.5	2.6
D1	3.4	4.2	4.3	4.3	4.1	4.3	4.6	4.6	4.6	4.7
2	6.0	15.0	16.0	60.0	18.0	22.0	15.0	15.0	3,300	14.0
3	51.0	65.0	66.0	125.0	62.0	65.0	67.0	67.0	69.0	72.0
4	5.5	7.2	7.5	6.8	6.3	6.6	6.8	7.0	12.0	8.5
E1	3.5	4.0	4.0	3.9	3.9	4.0	4.1	4.1	4.2	4.3
2	3.4	4.0	4.0	3.9	3.8	4.1	4.1	4.0	4.1	4.3
3	3.4	4.0	4.0	3.9	3.8	4.0	4.1	4.0	4.1	4.2
4	3.4	4.0	3.9	3.9	3.8	4.0	4.0	4.0	4.1	4.2
5	3.5	4.1	4.0	4.1	4.0	4.2	4.3	4.3	4.4	4.6
F1	50.5	80.0	72.0	72.0	54.0	56.0	58.0	58.0	58.0	60.0
2	50.5	60.0	68.0	66.0	66.0	67.0	69.0	69.0	70.0	80.0
3	80.5	68.0	84.0	88.0	90.0	83.0	67.0	67.0	76.0	77.0
4	50.5	58.0	57.0	57.0	56.0	57.0	59.0	59.0	62.0	71.0
5	50.5	55.0	56.0	53.0	52.0	53.0	55.0	54.0	55.0	66.0
G1	3.6	4.0	4.0	4.1	3.9	4.5	4.2	4.1	4.2	4.3
2	3.5	4.4	4.3	4.3	4.3	4.5	4.6	4.4	4.5	4.6
3	3.6	4.6	4.6	4.6	4.6	4.8	4.8	4.8	4.9	5.0
4	3.6	2.8	4.2	4.2	4.1	4.3	4.4	4.2	4.4	4.4
5	3.6	3.0	4.8	7.7	7.2	6.4	6.3	6.2	6.3	10.0
H1	1.6	2.0	1.9	1.9	1.8	1.9	2.0	1.9	2.0	2.1
2	1.6	2.0	2.0	1.9	1.8	2.0	2.1	2.0	2.0	2.1
3	1.7	2.0	2.0	2.0	1.9	2.0	2.1	2.0	2.1	2.1
4	1.7	2.0	2.0	2.1	1.9	2.0	2.1	2.0	2.1	2.1
5	1.7	2.2	2.0	2.0	1.9	2.0	2.1	2.0	2.1	2.1
K1	2.9	2.5	1,000	1,250	1,950	--	11,000	5,600	14,000	2,000
2	2.9	3.7	3.7	3.5	3.4	3.6	3.7	3.6	3.7	3.8
3	2.9	3.8	3.8	3.7	3.5	3.7	3.8	3.8	3.9	3.9
4	2.9	4.2	4.5	4.5	4.7	4.7	5.2	5.2	5.3	4.5
5	3.0	2.6	5.8	5.6	5.3	5.7	5.4	5.3	4.3	11.0

TABLE XI (Cont)
EFFECT ON ENVIRONMENTAL CYCLING ON CIRCUIT PERFORMANCE (Cont)
Board: 35 Substrate: Aluminum Vias: Gold Filled

Circuit	Resistance (ohms)									
			Cycles Completed, -55 to +100°C				Ditto, but at 90% R.H.			
	B.F.*	A.F.*	30	52	106	216	234	263	317	427
L1	1.2	1.7	1.7	1.6	1.4	1.5	1.6	1.7	1.6	1.7
2	1.2	1.7	1.7	1.6	1.7	1.6	1.7	1.6	1.7	1.7
3	1.3	1.7	1.7	1.6	1.5	1.6	1.7	1.7	1.7	1.8
4	1.3	1.5	1.7	1.6	1.5	1.6	1.6	1.6	1.7	1.8
5	1.3	1.5	1.7	1.6	1.6	1.6	1.7	1.7	1.7	1.7
M1	0.8	1.2	1.4	1.1	1.0	1.0	1.1	1.1	1.1	1.2
2	1.0	3.6	N.R.**	2,250	1,850	1,500	2,500	3.4	3.6	3.4
3	0.4	0.8	1.0	0.7	0.6	0.7	0.8	0.7	0.8	0.8
4	0.9	1.4	1.4	1.2	1.1	1.2	1.3	1.3	1.3	1.3
5	1.0	2.9	3.5	3.4	3.2	3.7	4.0	3.5	3.7	2.7
6	0.4	1.1	1.0	0.8	0.7	0.7	0.9	0.8	0.8	0.9
N1	1.0	1.5	1.8	1.7	1.4	1.5	1.6	1.6	1.7	1.8
2	1.4	7.0	7.0	7,600	4,800	7,500	8,700	9,500	10,000	11,000
3	0.5	2.9	76.0	3.8	67.0	130.0	5.5	3.1	3.9	3.9
4	1.0	1.5	1.7	1.5	1.3	1.3	1.5	1.4	1.4	1.6
5	1.2	20.0	62.0	35.0	11.5	450.0	3,000	9.0	9.2	7.8
6	0.5	110.0	22,000	67,000	60,000	40,000	600.0	110.0	1,000	2,000
P1-1	OK***	OK	OK	OK	OK	OK	OK	OK	OK	OK
2-2	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
3-3	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
4-4	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
5-5	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
6-6	OK	OK	OK	OK	1.7	1.6	1.5	1.7	1.7	1.8
7-7	--	OK	OK	OK	OK	OK	OK	OK	OK	OK
8-8	--	OK	OK	OK	OK	OK	OK	OK	OK	OK
GR1	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
2	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
(GR)P1-2	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
P5,3-4,6	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
P7-8	--	0.8	1.1	0.8	0.5	0.6	0.9	OK	OK	OK
R1	--	--	10.0	10.1	10.0	10.0	10.4	10.3	10.6	10.9
2	--	--	10.0	10.1	10.0	10.0	10.4	10.3	10.6	11.6
3	--	--	10.0	10.0	10.0	10.0	10.2	10.3	10.6	10.9
4	--	--	10.0	10.1	10.0	10.1	10.5	10.6	10.6	11.0

*B.F.: Before filling of vias; A.F.: After filling of vias, but before commencement of environmental cycling.

**No detectable reading. Impedance exceeds 5×10^7 ohms and circuit is presumed open.

***No detectable current leakage or dielectric failure.

TABLE XII
EFFECT OF ENVIRONMENTAL CYCLING ON CIRCUIT PERFORMANCE
Board: 14 Substrate: Vespel Vias: Organic

Circuit	Resistance (ohms)									
			Cycles Completed, -55 to +100°C				Ditto, but at 90% R.H.			
	B.F.*	A.F.*	30	52	106	216	234	263	317	427
A1	0.9	25.0	82.0	160.0	250.0	120.0	200.0	Damaged	--	--
2	1.2	1.0	1.3	1.2	1.2	1.3	1.5	1.6	1.6	2.1
3	1.2	1.0	1.2	1.2	1.1	1.2	5×10^5	1.9×10^5	1.5×10^5	1.1×10^5
4	2.0	2.0	2.2	2.2	2.1	2.3	53.0	46.0	64.0	3,800
B1	1.2	1.3	1.4	1.3	1.2	1.3	1.3	1.3	1.1	1.6
2	1.2	5.6	6.8	6.7	6.7	6.8	9.0	9.6	9.1	10.1
3	1.5	1.2	1.7	1.5	1.4	1.6	1.7	N.R.**	N.R.	N.R.
4	3.5	4.0	5.2	37.0	42.0	52.0	6,500	8,000	5×10^4	N.R.
C1	1.7	1.6	1.9	1.8	1.8	1.9	2.0	1.8	1.6	2.2
2	2.3	2.5	2.5	2.5	2.4	2.5	2.6	2.4	2.2	2.7
3	2.7	2.5	2.8	2.8	2.6	2.8	2.9	2.9	2.7	3.4
4	5.0	4.8	5.3	5.3	5.3	5.3	25.0	23.0	26.0	25.0
D1	3.5	3.3	3.6	3.6	3.5	3.6	4.0	38.0	45.0	42.0
2	4.2	18.0	38.0	49.0	62.0	27.0	800.0	900.0	1,000	1,000
3	6.5	6.5	7.2	7.2	7.3	11.5	8.0	9.0	2×10^4	5×10^4
4	13.0	12.0	13.5	14.6	13.5	18.0	N.R.	1×10^5	N.R.	N.R.
E1	12.0	11.0	11.7	11.6	11.5	11.6	12.0	12.0	13.0	14.0
2	12.0	11.0	11.1	11.1	11.7	11.3	11.0	11.8	2×10^5	N.R.
3	11.0	10.0	34.0	37.0	36.0	40.0	68.0	67.0	68.0	N.R.
4	N.R.	10.0	11.2	11.2	11.1	11.5	13.0	16.0	2×10^4	2×10^4
5	14.0	12.0	12.5	12.5	12.2	13.0	16.0	400.0	370.0	400
F1	4.8	4.4	5.0	4.9	4.7	4.8	4.8	4.9	4.9	7.0
2	4.8	4.6	4.9	4.8	4.7	4.8	4.7	4.8	5.2	7.5
3	6.5	4.4	4.9	4.7	4.6	4.7	4.8	5.0	5.2	N.R.
4	7.0	30.0	220.0	220.0	260.0	300.0	1,300	1,500	3×10^5	N.R.
5	5.5	4.4	7.0	150.0	30.0	9.0	N.R.	N.R.	N.R.	N.R.
G1	2.5	2.4	2.9	2.8	2.7	2.7	2.7	2.7	2.6	3.1
2	2.5	2.3	2.9	2.7	2.6	2.7	N.R.	N.R.	N.R.	5×10^5
3	2.4	2.5	3.0	2.9	2.7	2.9	6×10^4	N.R.	4×10^5	N.R.
4	3.0	2.4	2.9	2.9	2.6	2.7	7.0	6.6	5.9	N.R.
5	2.4	2.4	3.3	3.1	2.8	3.0	3.0	3.0	2.8	5.2
H1	2.3	6.0	7.2	6.8	6.8	7.0	7.5	1,100	1,600	2,500
2	2.3	2.1	3.0	2.6	2.6	2.6	2.5	2.5	2.1	2.6
3	2.3	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.
4	2.2	2.5	4.1	8.8	11.0	3.3	83.0	90.0	73.0	75.0
5	2.3	2.5	4.7	4.3	4.3	4.5	7,000	8×10^4	1.5×10^4	5×10^4
K1	2.4	2.5	2.2	2.4	2.2	2.2	2.3	2.3	2.1	2.8
2	2.1	2.3	2.3	2.3	2.2	2.2	2.1	2.2	1.9	2.2
3	2.1	1.9	2.3	2.3	2.2	2.1	2.2	2.2	1.9	2.2
4	2.0	1.8	2.3	2.3	2.2	2.2	2.1	2.4	2.5	3.1
5	2.0	1.9	2.2	2.3	2.2	2.2	2.2	2.2	2.0	2.5

TABLE XII
EFFECT OF ENVIRONMENTAL CYCLING ON CIRCUIT PERFORMANCE (Cont)
Board: 14 Substrate: Vespel · Vias: Organic

Circuit	Resistance (ohms)									
			Cycles Completed, -55 to +100°C				Ditto, but 90% R.H.			
	B.F.*	A.F.*	30	52	106	216	234	263	317	427
L1	1.9	9.0	82.0	94.0	67.0	100.0	200.0	2.1×10^4	4×10^4	$.7 \times 10^4$
2	1.9	1.7	2.3	2.2	2.2	2.1	2.5	2.7	2.5	3.1
3	1.9	1.7	2.4	2.1	2.1	2.1	2.2	14.0	350.0	390.0
4	1.9	20.0	1,200	3,700	3,700	1.5×10^5	N.R.	N.R.	N.R.	N.R.
5	1.9	14.0	55.0	52.0	58.0	67.0	1,200	2,300	2,000	2,400
M1	1.1	2.0	2.3	2.3	2.6	2.5	2.2	2.0	1.8	2.2
2	3.5	50.0	120.0	135.0	160.0	165.0	800.0	750.0	800.0	1,000
3	1.8	1.9	1.9	1.9	2.3	3.4	75.0	100.0	100.0	120.0
4	1.1	2.5	2.8	2.9	2.6	2.8	3.0	2.8	2.5	2.7
5	1.1	2.7	2.8	3.5	3.3	3.5	2.3	2.4	2.2	2.6
6	1.7	1.6	1.4	1.4	1.3	1.4	1.4	1.4	1.4	95.0
N1	1.0	2.8	4.1	4.3	4.3	4.6	4.6	4.2	3.8	4.4
2	1.3	30.0	62.0	66.0	67.0	78.0	68.0	65.0	57.0	110.0
3	3.2	85.0	360.0	420.0	480.0	500.0	500.0	550.0	750.0	1,000
4	0.9	7.0	13.2	14.5	16.5	23.0	37.0	28.0	24.0	38.0
5	1.5	14.0	17.5	19.0	17.5	17.5	19.0	17.0	15.0	16.0
6	2.3	3.5	2.1	2.2	2.1	2.2	2.4	2.6	60.0	350.0
P1-1	OK***	OK	OK	OK	OK	OK	OK	OK	OK	OK
2-2	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
3-3	2.5	3.5	2.1	1.7	1.7	1.8	1.8	1.8	1.8	2.5
4-4	1.9	2.0	0.9	0.9	0.9	1.0	1.0	1.1	1.0	1.7
5-5	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
6-6	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
7-7	--	OK	OK	OK	OK	OK	OK	OK	OK	OK
8-8	--	OK	OK	OK	OK	OK	OK	OK	OK	OK
GR1	--	--	--	--	--	--	--	--	--	--
2	--	--	--	--	--	--	--	--	--	--
(GR)P1-2	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
P5,3-4,6	2.3	3.0	2.3	2.2	2.0	2.0	2.0	2.0	1.8	2.1
P7-8	--	OK	OK	OK	OK	OK	OK	OK	OK	OK
R1	--	--	10.5	10.3	10.2	10.2	11.5	16.0	N.R.	N.R.
2	--	Lost	--	--	--	--	--	--	--	--
3	--	--	10.5	10.3	10.2	10.4	10.3	10.3	10.1	10.5
4	--	--	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.

*B.F.: Before filling of vias; A.F.: After filling of vias, but before commencement of environmental cycling.

**No detectable readings. Impedance exceeds 5×10^7 ohms and circuit is presumed open.

***No detectable current leakage or dielectric failure.

TABLE XIII
EFFECT OF ENVRIONMENTAL CYCLING ON CIRCUIT PERFORMANCE
Board: 11 Substrate: Vespel Vias: Gold Filled

Circuit	Resistance (ohms)									
			Cycles Completed, -55 to +100°C				Ditto, but at 90% R.H.			
	B.F.*	A.F.*	30	52	106	216	234	263	317	427
A1	2.3	3.5	3.0	2.4	2.3	2.6	2.7	2.8	2.9	4.8
2	2.8	2.5	2.3	1.6	1.5	1.7	1.9	1.9	2.2	2.7
3	0.9	1.4	1.1	0.7	0.7	0.7	0.8	0.8	0.8	1.1
4	0.8	1.9	1.4	1.1	1.1	1.3	1.2	1.4	1.5	1.9
B1	3.6	4.4	3.7	3.6	3.6	3.6	3.7	3.6	3.8	4.0
2	3.0	3.0	2.5	2.4	2.4	2.4	2.5	2.5	2.5	2.7
3	0.9	1.2	2.5		370.0	30.0	120.0	116.0	1.8	3.0
4	1.3	1.5	1.8	1.5	1.5	1.5	1.7	1.7	1.8	2.1
C1	6.0	7.0	6.5	6.3	6.2	6.2	6.5	6.3	6.3	6.5
2	7.5	5.0	4.6	4.2	4.1	4.1	4.5	4.4	4.4	4.6
3	1.7	2.3	2.1	1.7	1.6	1.7	1.8	1.8	2.1	2.3
4	2.4	3.1	2.9	2.6	2.5	2.6	2.8	2.9	3.3	4.6
D1	11.0	12.0	11.8	11.8	11.5	11.5	11.0	12.0	12.0	12.5
2	8.0	8.5	8.4	8.2	8.2	8.1	8.6	8.5	9.0	17.0
3	3.0	4.0	3.3	3.0	3.0	3.0	3.6	4.6	85.0	12.0
4	7.0	8.0	7.7	7.6	7.5	7.5	8.0	8.0	8.4	9.6
E1	6.0	7.5	6.4	6.1	6.1	6.2	7.0	6.9	6.9	8.6
2	15.0	7.5	6.3	5.9	5.9	6.0	6.7	6.9	7.1	7.8
3	5.5	7.5	6.2	5.9	5.8	6.0	6.7	6.9	8.0	N.R.
4	5.5	6.0	6.3	6.2	6.2	6.2	6.7	7.1	9.0	12.0
5	5.5	7.0	8.7	78.0	115.0	3.6	250.0	1,000	2,800	N.R.
F1	2.2	2.6	2.8	2.5	2.3	2.4	2.7	2.5	2.6	N.R.
2	2.2	2.5	2.8	2.4	2.3	2.3	2.7	2.5	2.9	3.2
3	2.9	3.7	N.R.**	200.0	8,500	250.0	$4x10^4$	500.0	N.R.	$3x10^4$
4	N.R.	7.2	2,300	1,450	135.0	200.0	700.0	1,800	2,700	3,100
5	3.6	3.7	3.9	3.7	3.6	3.6	4.0	4.4	8.0	N.R.
G1	5.0	5.2	5.5	5.3	5.3	5.3	5.7	5.5	6.6	5.5
2	6.0	5.1	5.3	5.2	5.2	5.1	5.5	5.3	5.3	5.5
3	10.0	5.4	5.6	5.4	5.4	5.4	6.0	6.0	6.0	6.2
4	10.0	4.5	4.8	4.7	5.7	5.8	4,200	5,500	7.0	8.0
5	6.5	4.5	4.7	4.6	5.5	5.6	5.9	5.8	5.9	6.0
H1	8.0	6.0	5.8	5.7	5.7	5.7	6.0	5.6	8.4	8.4
2	8.0	6.0	6.1	5.8	5.8	5.8	6.3	5.8	8.8	9.0
3	7.5	8.5	8.3	8.4	8.3	8.2	8.7	8.0	7.4	8.5
4	7.5	8.0	7.8	7.9	7.7	7.7	8.2	7.5	7.9	8.2
5	7.5	8.0	7.7	7.7	7.6	8.0	7.9	7.5	7.7	7.8
K1	4.2	7.5	4.1	3.9	3.8	3.8	4.3	4.0	5.3	5.3
2	4.6	4.8	4.5	4.5	4.3	4.2	4.7	4.4	5.9	6.4
3	4.4	4.5	4.8	4.6	4.5	4.4	4.9	4.7	5.0	5.6
4	12.0	4.5	5.1	4.9	4.9	4.9	8.0	8.0	8.3	8.5
5	5.0	5.4	6.0	5.7	5.5	5.5	6.2	6.0	6.4	6.6

TABLE XIII
EFFECT OF ENVIRONMENTAL CYCLING ON CIRCUIT PERFORMANCE (Cont)
Board: 11 Substrate: Vespel Vias: Gold Filled

Circuit	Resistance (ohms)									
			Cycles Completed, -55 to +100°C				Ditto, but at 90% R.H.			
	B.F.*	A.F.*	30	52	106	216	234	263	317	427
L1	8.0	8.5	7.7	7.4	7.3	7.3	8.3	8.0	9.0	$9x10^4$
2	7.5	8.5	7.4	6.8	6.8	6.8	8.4	11.0	12.0	25.0
3	6.5	8.0	7.5	7.1	6.9	7.0	7.9	9.5	10.2	10.0
4	11.0	8.0	7.3	6.8	10.2	10.2	12.0	11.5	14.3	6,500
5	6.0	7.0	6.6	22.0	22.0	22.0	4,200	5,500	27.0	6,500
M1	3.5	4.4	34.0	150.0	5.3	180.0	85.0	115.0	135.0	700.0
2	1.5	2,000	$4.5x10^4$	$3.5x10^4$	$4.3x10^4$	200.0	2,500	$4x10^4$	$5x10^4$	10.0
3	0.8	35.0	2.2	1.8	1.8	1.6	1.8	1.8	2.5	15.0
4	3.6	3.4	3.9	3.6	3.6	3.6	4.6	5.5	6.5	145.0
5	1.5	1,000	94.0	62.0	58.0	1.9	2.1	5.0	3.6	6.0
6	0.8	1.2	1.6	1.1	1.1	1.1	2.0	2.4	3.0	35.0
N1	4.0	4.6	4.5	4.2	4.2	4.2	4.4	4.2	4.3	4.4
2	2.2	2.8	2.8	2.3	2.3	2.3	2.4	2.3	2.4	2.6
3	1.1	2.8	3.4	3.5	2.6	2.6	3.8	2.3	3.4	4.0
4	3.4	4.6	3.9	3.6	3.5	3.5	3.7	3.5	3.7	3.9
5	2.8	2.8	2.3	1.9	1.9	1.9	2.1	2.4	2.9	3.5
6	1.1	2.5	1.9	1.3	1.4	1.3	1.5	1.7	1.7	1.9
P1-1	OK***	OK	OK	OK	OK	OK	OK	OK	OK	OK
2-2	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
3-3	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
4-4	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
5-5	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
6-6	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
7-7	--	OK	OK	OK	OK	OK	OK	OK	OK	OK
8-8	--	OK	OK	OK	OK	OK	OK	OK	OK	OK
GR1	--	--	--	--	--	--	--	--	--	--
2	--	--	--	--	--	--	--	--	--	--
(GR)P1-2	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
P5,3-4,6	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
P7-8	--	OK	OK	OK	OK	OK	OK	OK	OK	OK
R1	--	--	10.7	10.9	10.2	10.5	N.R.	N.R.	N.R.	N.R.
2	--	--	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.
3	--	--	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.	N.R.
4	--	--	10.5	10.4	10.2	10.1	Lost	--	--	--

*B.F.: Before filling of vias; A.F.: After filling of vias, but before commencement of environmental cycling.

**No detectable readings. Impedance exceeds 5 x 10^7 ohms and circuit is presumed open.

***No detectable current leakage or dielectric failure.

The base-line values are listed in the column headed "AF" and serve as 0-cycle readings for the environmental stress data following. The column headed "216" also is equivalent to the 0-cycle starting point for the high humidity test results listed to the right. However, in the high humidity series, as in the "normal" humidity series, "failure" is defined only on the base-line values in column "AF".

Initial Summary of Results. – A superficial examination of the data listed in these tables suggests that stable circuit performance is well within the bounds of the technology under development but that much yet needs to be done in optimizing process techniques to achieve a favorable yield factor. Although not directly measured, the compatibility of the materials used in this process appears to be borne out by the results.

A comparison of "BF" and "AF" entries indicates that inoculation with z-direction conductor may produce either an increase or a decrease in resistance. On a single board this may equal or exceed 25 percent of the average "BF" value. An increase in resistance normally would be expected since the conductor applications (including the "T" layer metallization) add further elements to the original conductive path. A persistent decrease, particularly of the size exhibited by Board 31 (Table IX), therefore requires some interpretation. It is possible that probe contacts to the gold metallizations in the "BF" series of measurements on this board were generally faulty due to possible etching damage to the gold. Filling with z-direction conductor could be assumed to establish more intimate, and larger area, contact with these metallizations than was achieved in probing. Another possibility is that the metallizations in Board 31 were consistently thinner than in most of the other boards, again leading to reduced electrical contact on "BF" probing. This seems unlikely, however, because each metallization is independently deposited, which would lead to a dependence of resistance change on circuit level. Such a dependence does not appear to be supported by the data. A third possibility is the presence of a systematic operator error which was reduced, or eliminated, in subsequent sets of measurements. The first set of measurements taken was the "BF" series on Board 31; services of the same operator were employed on all succeeding measurements. A more detailed analysis of the data may yield further insight into the origin of this reduction of electrical resistance following completion of the last four fabrication steps.

Board 11 on Vespel also showed a slight tendency toward a negative resistance increment between "BF" and "AF" readings. The trend is somewhat obscured by a few anomalously high readings and is considerably less general than that in Board 31. The degree of significance here will depend on further analysis. If the effect actually is significant on Board 11, a correlation either with substrate material or with z-direction conductor material would appear to be ruled out.

Also of process interest are the absolute values of the resistance increments. Examination of the data from the remaining three boards (No.'s 36, 35 and 14; Tables X, XI and XII) reveals a positive increment of the order of 1.6 ohms, or 0.8 ohms per via, if the data from highly failure-prone circuits (i.e., circuits that failed after the first 30 thermal cycles) are excluded. This would appear to be a tolerable via resistance for a great majority of multilayer board applications. Of second order importance are the correlations of via resistance with cross-section, depth and z-direction conductor material. It will be recalled that gold-filled conductor

materials have tended to exhibit resistances higher than the organic-filled materials, possibly because of skin effects. This trend is perpetuated in the three boards under consideration, the average resistance increment being distinctly higher in Board 35 (Table XI) than in the other two boards.

In the succeeding exposure of the boards to 427 environmental stress cycles another distinct grouping of data emerged. This was the set of current leakage tests across dielectric regions, including capacitor dielectrics, line-spacings, and leakage-to-ground. In marked contrast to the conductive paths, the dielectric displayed a remarkable immunity to the cycling in all categories. In a total of 61 test sites only one new failure appeared and another recovered, both on Board 35 (Table XI), for a net change of zero defects in an original total of eight. Of probable significance is the fact that the single recovery occurred to a line-spacing defect situated in the "T" layer where environmental stresses could exert a prominent effect on surface contamination or foreign bodies. The recovery was observed after the first 18 cycles at 90 percent relative humidity and appeared to be permanent.

At the termination of environmental stress exposure six of the defects were found to be associated with capacitor dielectrics involving a total plate area of 225 cm^2. Assuming each defect to be due to only one breach in the dielectric, the resulting defect density in the total capacitor area was 0.024 cm^{-2}.

The terminal line-spacing defect count (10 mil conductor separation) was two in a total spacing length of 137 cm. Assuming again that each defect was due to a single discontinuity, the defect frequency was 0.015 cm^{-1}.

Another distinct group of data pertains to the resistors soldered to the boards prior to thermal cycling. As previously indicated, difficulty in soldering the resistors to Vespel boards led to the expectation of a high mortality rate during environmental stressing. This proved to be true. Of eight resistor sites on the two Vespel boards four were functional at the beginning of stress exposure and only one at the end. On the three aluminum boards, however, all twelve resistors were functional both initially and after the exposure. The resistance measurements invariably confirmed on all boards the nominal 10-ohm values except immediately prior to functional or physical loss. Probe contact in these measurements was made on contiguous conductor lines in order to include the solder connection entirely. Minor modifications in processing and soldering technique, as suggested earlier, should be capable of resolving the problem of component soldering to Vespel boards.

The remaining bloc of data pertains to the resistance of conductive paths. Applying the definition of failure given above (see page 39), it is immediately evident that degradation of electrical function occurs in a significant number of circuits as a result of thermal cycling, particularly at high humidity. In fact, the incidence of failures is almost five times as great at 90 percent than at 50 to 65 percent relative humidity. The data are summarized in Table XIV.

TABLE XIV
CIRCUIT FAILURES INDUCED BY THERMAL CYCLES AT AMBIENT AND AT HIGH HUMIDITY

Substrate	Board Number	Z-direction Conductor	Circuits Initially Functional	Failures After 216 Cycles	Failures Added at 90% R. H. (211 cycles)	Total Failures
Aluminum	31	Organic	58	0	11	11
Aluminum	36	Organic	56	1	12	13
Aluminum	35	Gold	56	7	-2	5
Vespel	14	Organic	50	5	24	29
Vespel	11	Gold	55	2	11	13
Totals			275	15	56	71

The results show that the toll is about five percent of the initially functional circuits at the more moderate humidity condition and about 20 percent at high humidity. Since the effects should be additive, exposure of the initial boards to high humidity alone would have caused 26 percent of the initially functional circuits to fail.

On the aluminum boards a total of 17 percent of the 170 originally functional circuits failed. On Vespel the total was 40 percent of an original 105 circuits. Omitting the terminal high humidity exposure, however, the corresponding proportions are 4.7 percent on aluminum and 6.0 percent on Vespel. The origin of the disparity appears, therefore, to lie in the effects of humidity which are almost three times more severe on the Vespel boards than on the aluminum boards. These effects probably arise from the permeability of the Vespel to water, which may cause mechanical stresses on the circuits and their vias through dimensional changes. Such dimensional changes could be expected particularly at the cold end of the cycle (which reaches -55 deg C) where water already absorbed in the Vespel would become frozen and expand. The aluminum boards, being impervious, would not be subject to this type of mechanical flexing.

A further differentiating factor between the aluminum and Vespel boards may lie in the greater experience gained with the aluminum (37 fabrication starts as opposed to only 17 on Vespel) and the inherently greater processing reliability gained therefrom.

Also deducible from Table XIV is an over-all comparison of organic-filled and gold-filled z-direction conductor performance under stress. From the final totals 32 percent of the originally functional circuits with organic-filled conductors failed as compared with 16 percent with the gold-filled conductors. Again, however, the main departure occurred in the high humidity cycling. Prior to this point, of the initially functional circuits only 3.7 percent failed among the organic-filled group whereas 8.1 percent failed among the gold-filled group. Thus, in the high humidity treatment the organic-filled failures increased by a factor of almost nine, but the gold-filled only by a factor of two. A more exact and graphical representation of these effects is given in the next section.

Superficially the results appear to suggest a synergism between the organic materials (substrates and conductors) which predisposes them to a kind of disorganization under highly humid conditions. The highest increment of circuit failures suffered during the 90 percent relative humidity treatment occurred to Board 14 (Vespel substrate, organic-filled z-direction conductors) and amounted to 38 percent of the initially functional circuits. The corresponding figure was only half this value for the closest companion boards (31 and 36) which also had organic-filled conductors but aluminum substrates. Perhaps even more dramatic is the fate of the slotted plastic end-pieces of the holder (Figures 17 and 18) used to support the boards during cycling. The irreversible distortion is clearly evident and occurred primarily in the high humidity sequence. There was no visible evidence of distortion of the boards themselves, including those on Vespel.

Judgement on the selection and mode of application of organic materials in this process should not be passed, however, without a better understanding of the mechanisms(s) of failure. A contributing factor may be the metallizations themselves, particularly the adhesive bond between the gold and polyimide layers. The previously

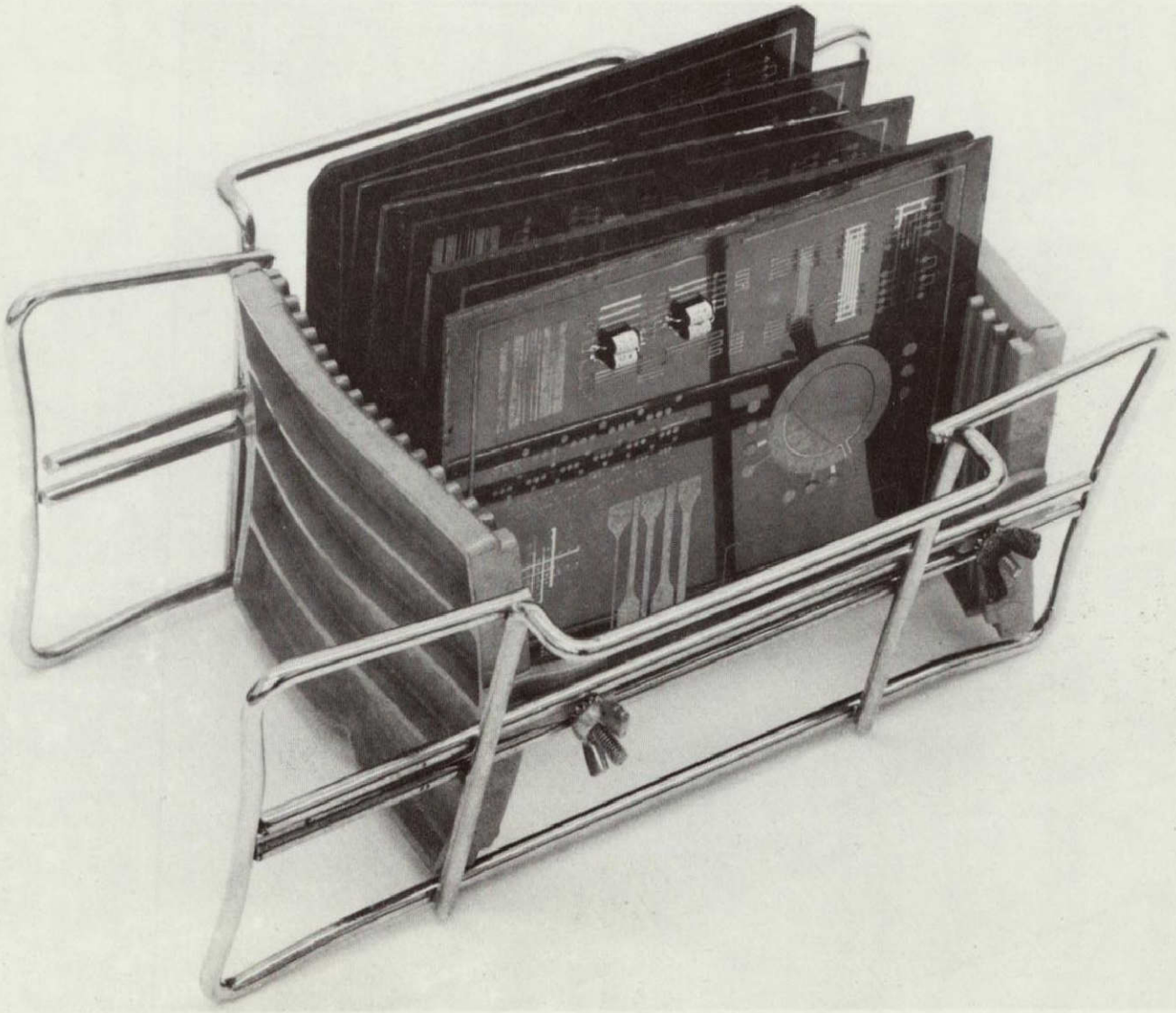


Figure 17. Distortion of Board Holder Due to Environmental Stress
(The Boards Themselves Suffered No Visible Distortion)

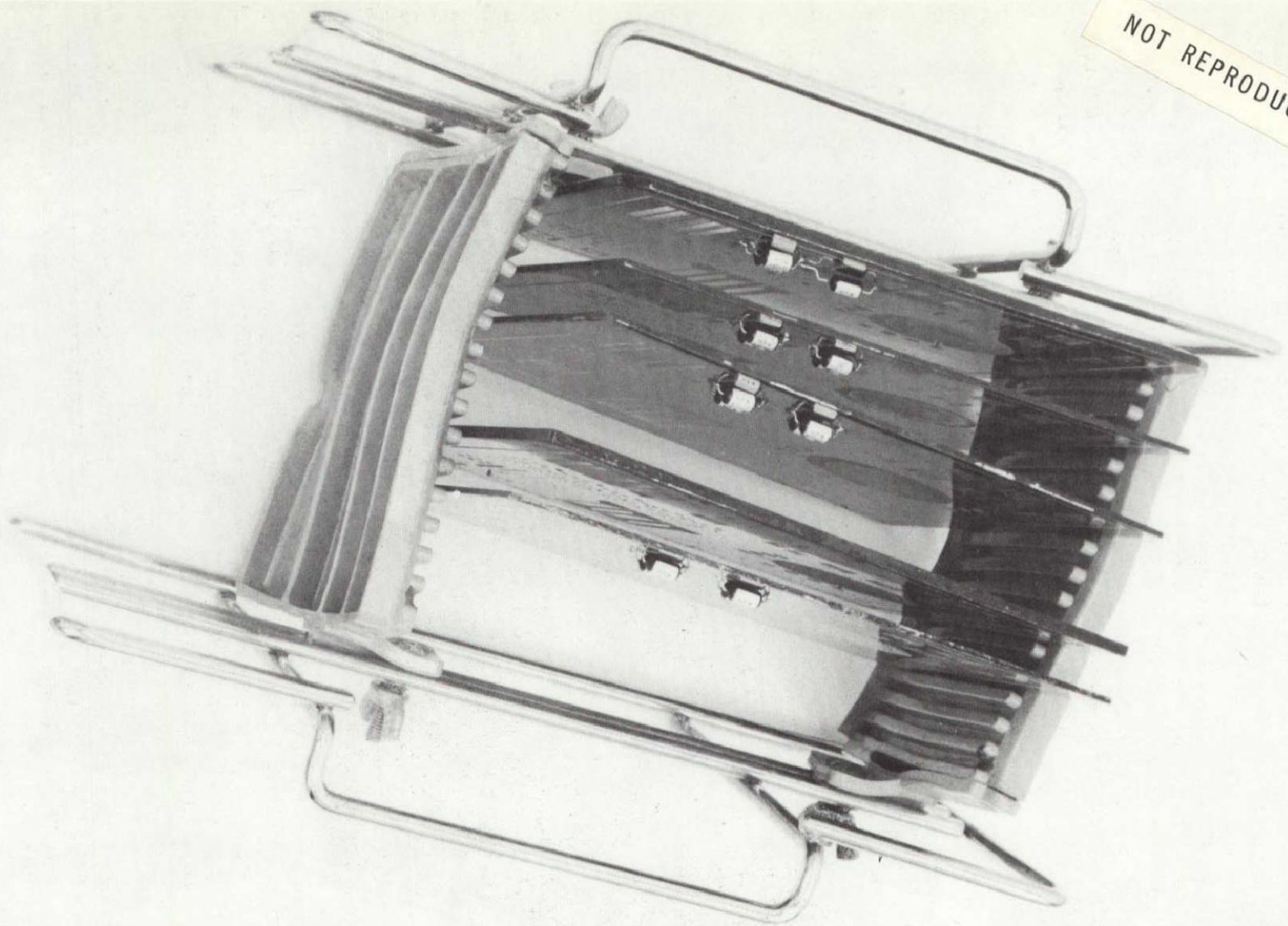


Figure 18. Distortion of Board Holder Due to Environmental Stress (Overhead View)

referenced problem of blistering almost always involved gold metallizations – principally those in the large capacitor areas. With the expansion of freezing water contained in a chilled plastic it is not difficult to imagine a simultaneous disengagement with an adjacent gold layer. Although not included in the present investigation it would be useful to carry out a matching environmental exposure on samples of conventional epoxy-glass boards for comparative purposes. Another interesting experiment would be to metallize the outer surfaces of a board (on Vespel and with organic-filled z-direction conductors) prior to high humidity cycling. Prevention of water transfer to and from the organic system by the metal coating could have a decisive influence on the performance longevity of the circuits. Most interesting, however, would be the extension of the use of the organic-filled conductor to the x, y – planes, thereby creating (on Vespel) a completely organic system in which gold/polymer interfaces are absent. Such a system should be much less humidity-sensitive since moisture sorption would be similar, and have matching effects, even if frozen, in all regions of the board.

Finally, it should be noted that 204 of the initially functional 275 circuits survived the entire environmental stress regime without significant change in their electrical characteristics. The substrate materials and z-direction conductor materials utilized in this group encompass all four combinations investigated on this program. Their functional durability throughout a two-month environmental stress regime bespeaks a significant compatibility among the materials employed and a sound approach to the use of these materials in an as yet embryo multilayer board technology.

Analysis of Circuit Function in Terms of Processing

The foregoing conclusions were substantiated in a more comprehensive manner by a statistical evaluation of the data listed in Tables IX, X, XI, XII, and XIII. Additional conclusions of process significance also were brought to light by this treatment. The test data were organized according to a 2 x 2 x 2 x 4 x 4 factorial design to evaluate the effects of thermal and high-humidity-thermal cycling on the variables: substrate material, interconnect via material, conductor line width and circuit layer level. The data consisted of the resistance readings (in ohms) taken before and during set stress cycle intervals as tabulated above.

The data were first treated by removing failed resistance paths from the overall treatment. A failure, as previously indicated, was arbitrarily defined as an increase in resistance to at least twice the base-line reading. The failure data were used separately to establish failure rates (expressed as failures per environmental stress cycle) as a function of substrate material, via material, line width and circuit level.

The remaining data (on good resistance paths) were subjected to computation of mean and standard deviation as a function of the characteristic being analyzed (e.g., via material, line width, etc.). The computations utilized the normal sums of squares techniques as follows:

$$\Sigma x_{ij} \quad \text{and} \quad \Sigma x_{ij}^2$$

where x_{ij} is the i^{th} resistance reading for the j^{th} characteristic.

The results of the statistical treatment of the data are plotted for quick trend review. All plots compare the characteristic being evaluated over a thermal cycling and a high-humidity-thermal cycling range and are presented in Figures 19 through 37. These plots are normalized so that they can be compared on an increase – decrease variance basis only.

Figure 19 shows the effects of thermal cycling on boards with aluminum substrates and Vespel substrates. Resistance values on the aluminum substrates tend to increase uniformly as a function of thermal cycles while those on the Vespel substrates decrease. The circuits on the Vespel substrates appear to be reaching a stabilization point while none is evident for those on aluminum.

Figure 20 plots the same variables under high-humidity-thermal cycling. The more pronounced effect with respect to Vespel is indicated. Of particular concern is the increase in slope after 100 cycles for the Vespel while aluminum tends to level off. The contrasting results indicated in Figures 19 and 20 most certainly are derived from the moisture permeability of the Vespel.

The effects of thermal cycling on organic-filled and gold-filled vias are shown in Figure 21. The pronounced negative slope for the gold filled vias suggests the use of thermal cycling as a conditioning screen for these boards. The physical significance of this trend is not immediately evident, although it probably is associated with a progressive inter-particle rupture of adhesive films under repeated thermal expansion and contraction.

With the introduction of 90 percent relative humidity a marked reversal in behavior of the two via materials occurs as seen in Figure 22. Resistance of both z-direction conductors increases with cycling, but the gold-filled paths increase in resistance at a much greater rate than the organic-filled. This result may indicate a negative compatibility factor applicable to the gold-filled conductor in relation to its dielectric and conductor line interfaces. The gold cannot absorb water and change its dimensions to correspond to the surrounding water-permeable media.

The effects of temperature cycling on resistance variance as a function of layer depth on aluminum substrates are shown in Figure 23. Recalling that Level 5 is closest to the substrate, and Level 2, closest to the top surface, it would appear that no layer-level-dependent trend exists.

The situation is quite different under high-humidity-thermal cycling, as shown in Figure 24 for aluminum substrates. Here the topmost buried layer accommodates well to the stress with a slight negative variance. Proceeding uniformly to deeper levels, however, one finds a progressive increase in circuit resistance associated with this accommodation. This appears to indicate another instance of negative materials compatibility. The aluminum substrate offers an impermeable barrier to moisture penetration, therefore it cannot respond to the dimensional changes occurring in the adjacent dielectric as a result of water absorption. Since the polyimide dielectric is deformable and essentially monolithic (except where interrupted by circuit layers) its accommodation to the dimensional mismatch with the substrate should follow a z-direction gradient. This is borne out in the trend shown in Figure 24: Full accommodation appears to set in after 100 cycles.

Continuing with boards on aluminum substrates, it is apparent from Figure 25 that thermal cycling, as expected, has the least effect on resistance variance

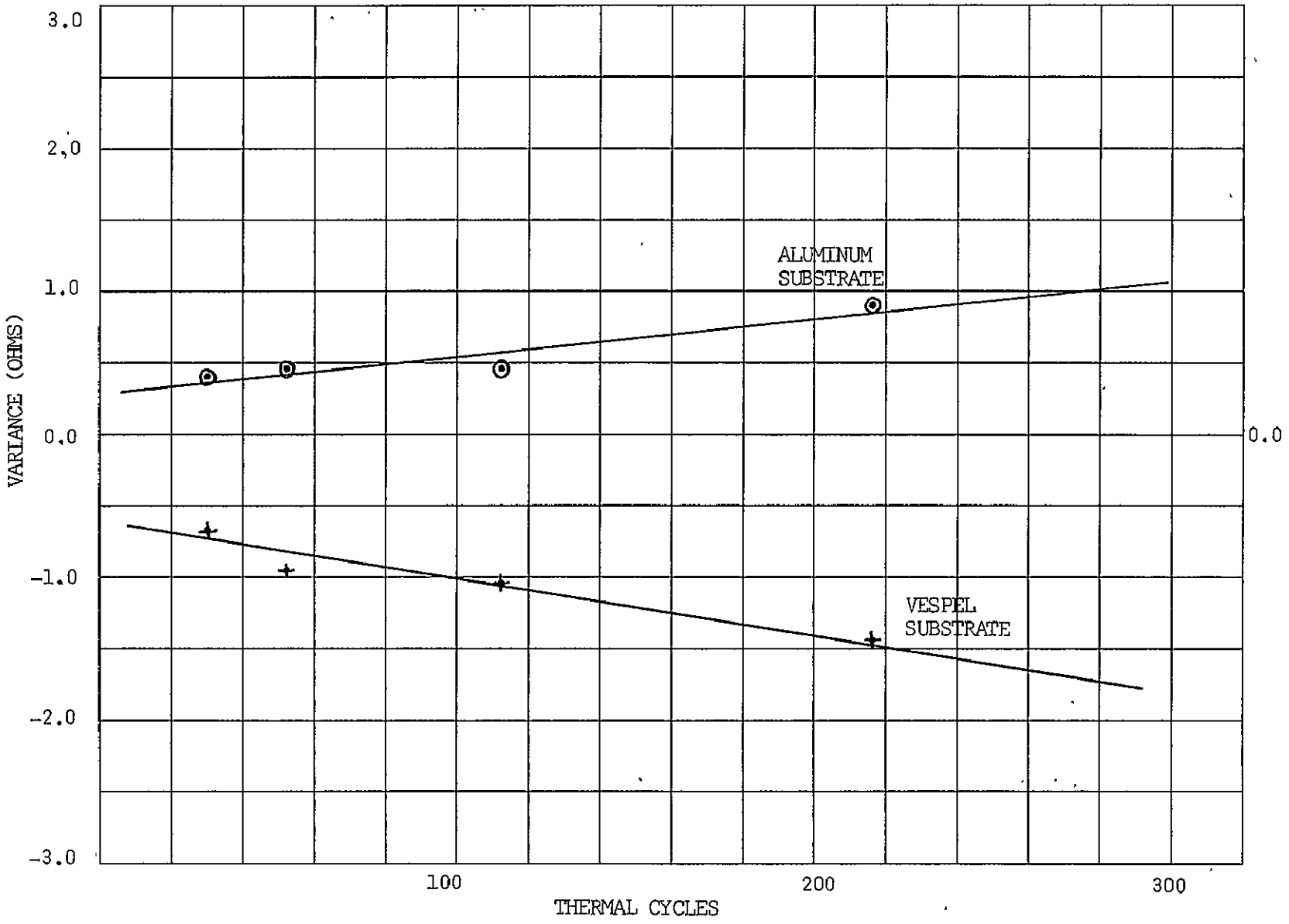


Figure 19. Temperature Effects vs. Substrate Material

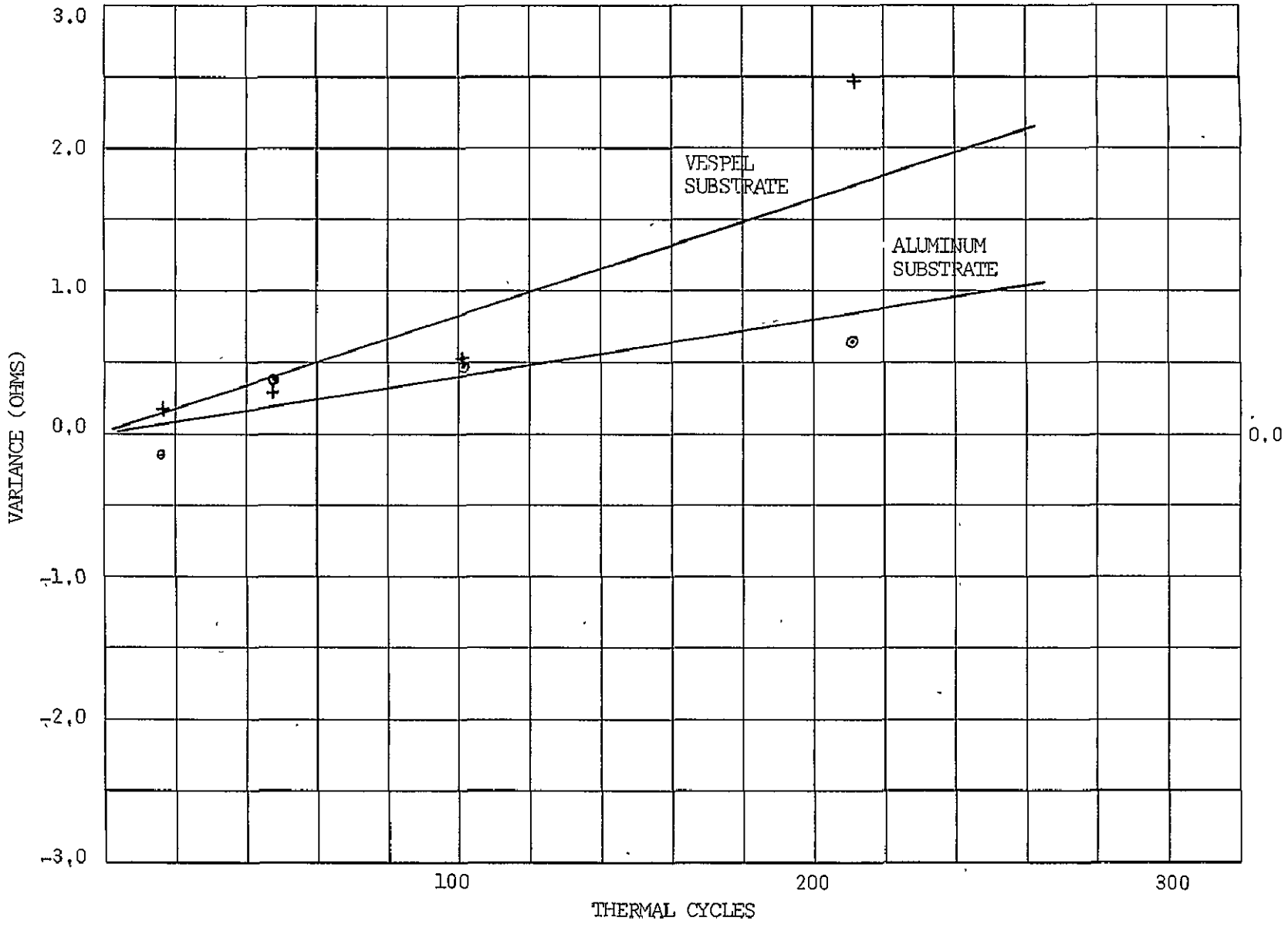


Figure 20. Humidity Effects vs. Substrate Material

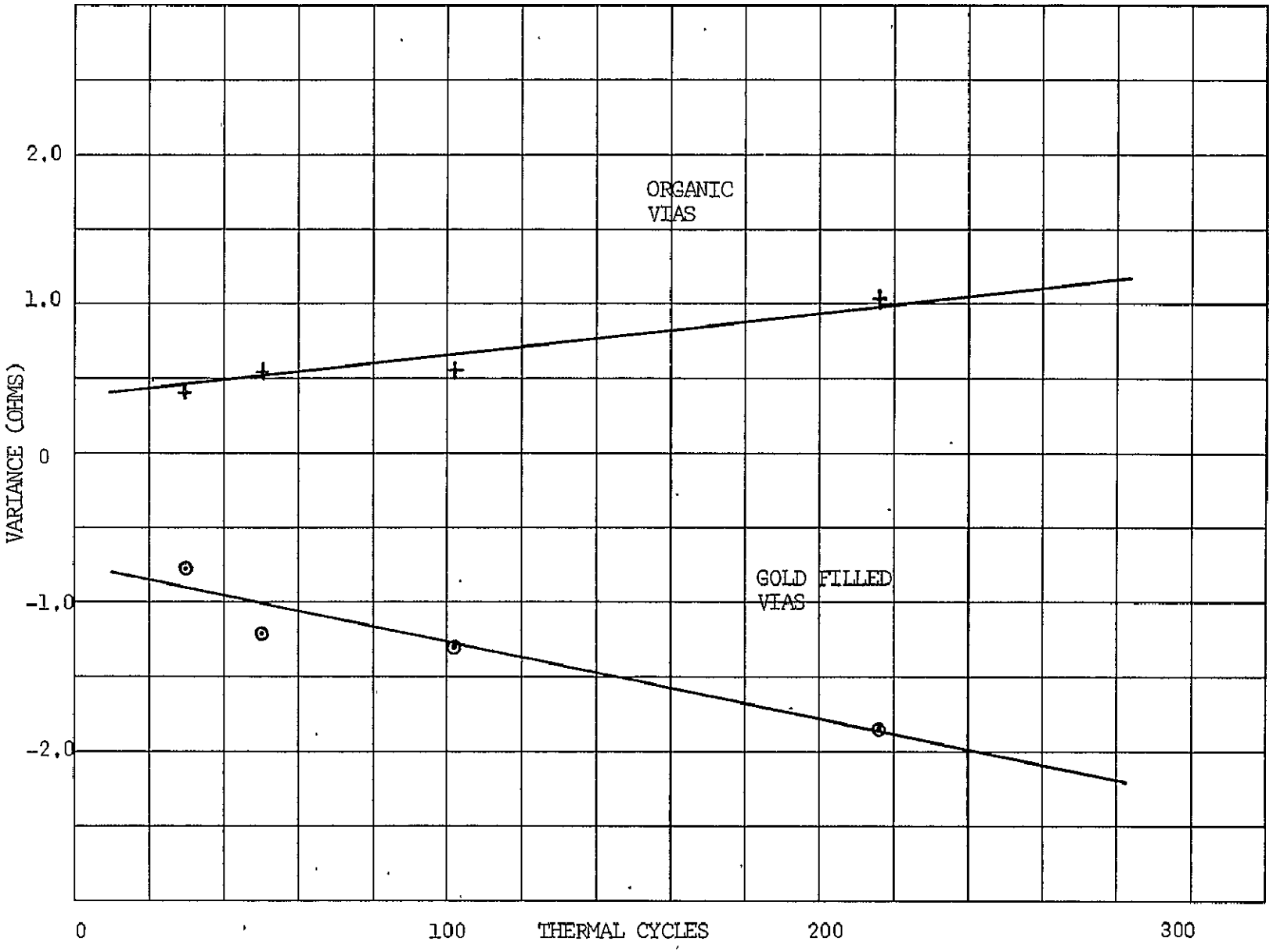


Figure 21. Temperature Effects vs. Via Material

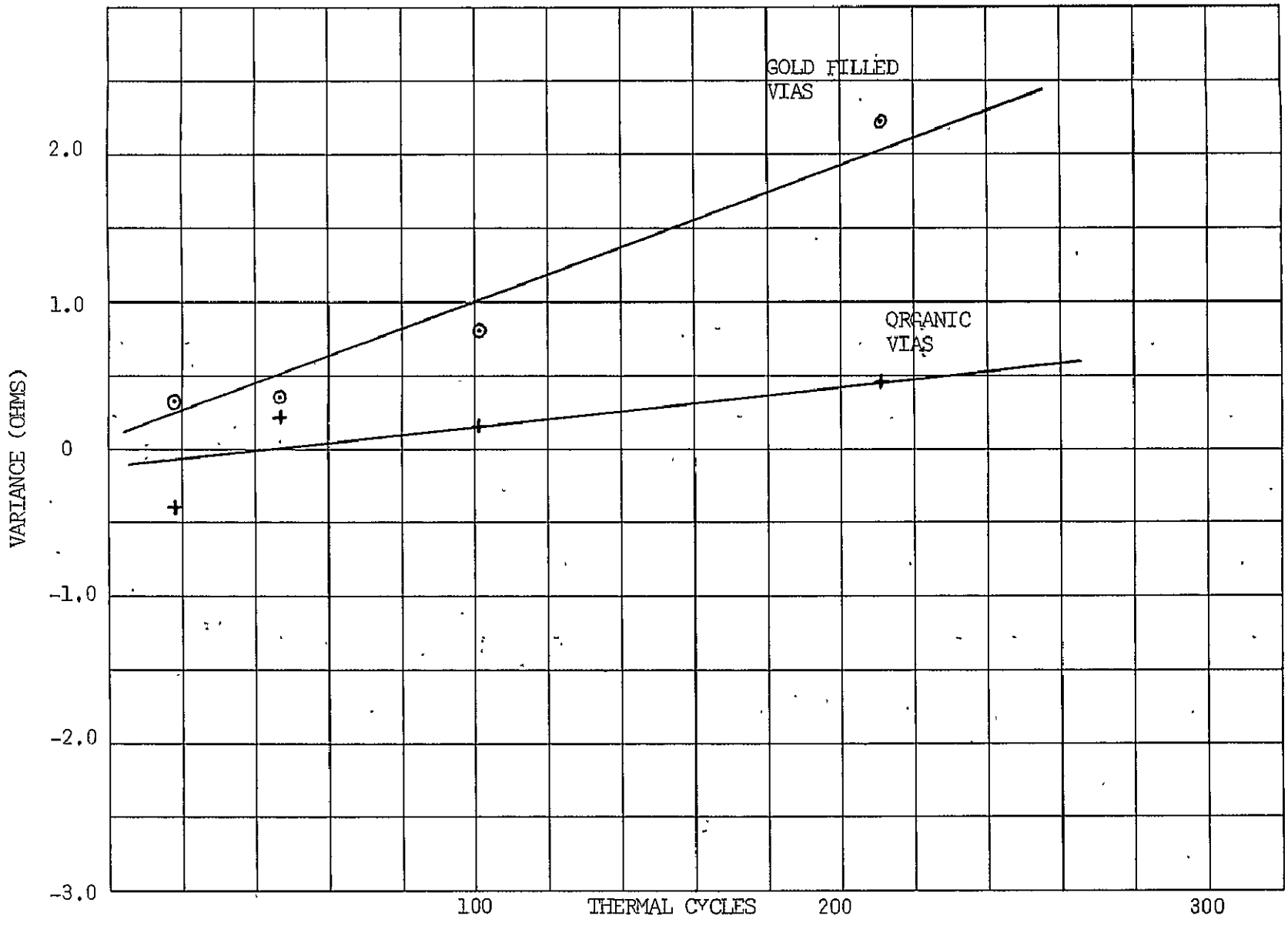


Figure 22. Humidity Effects vs. Via Material

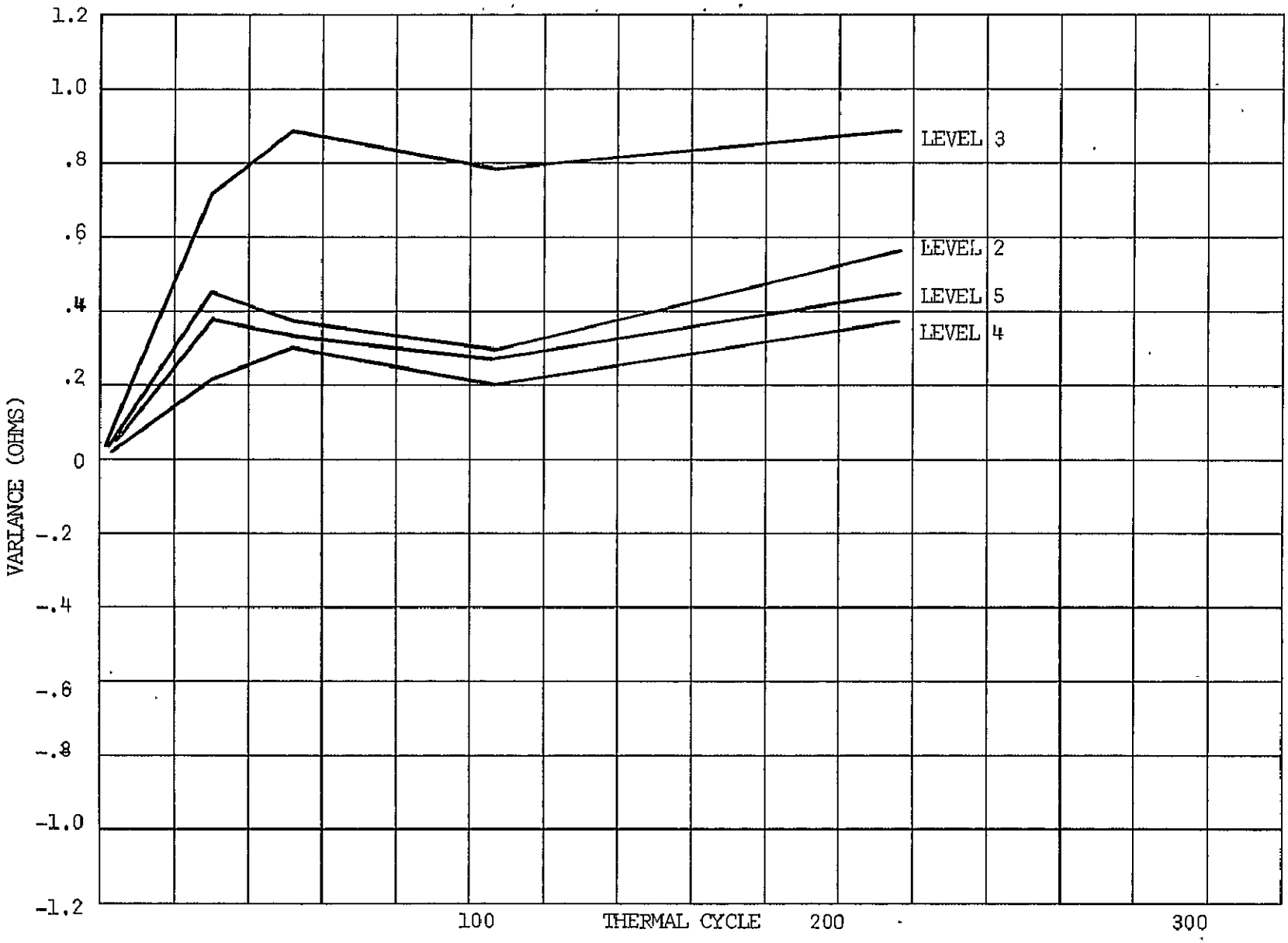


Figure 23. Temperature Effects vs. Layer Depth (Aluminum Substrate)

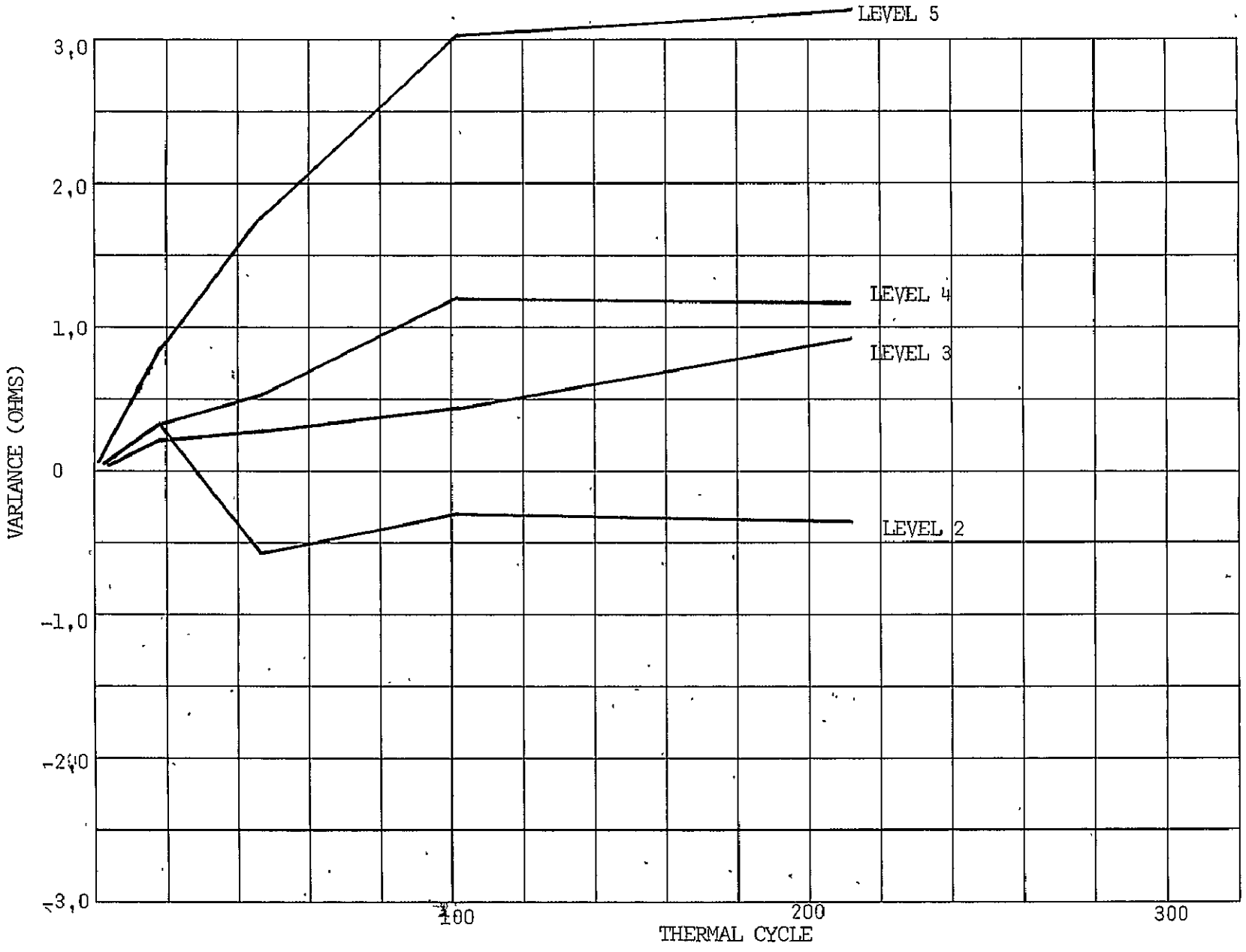


Figure 24. Humidity Effects vs. Layer Depth (Aluminum Substrate)

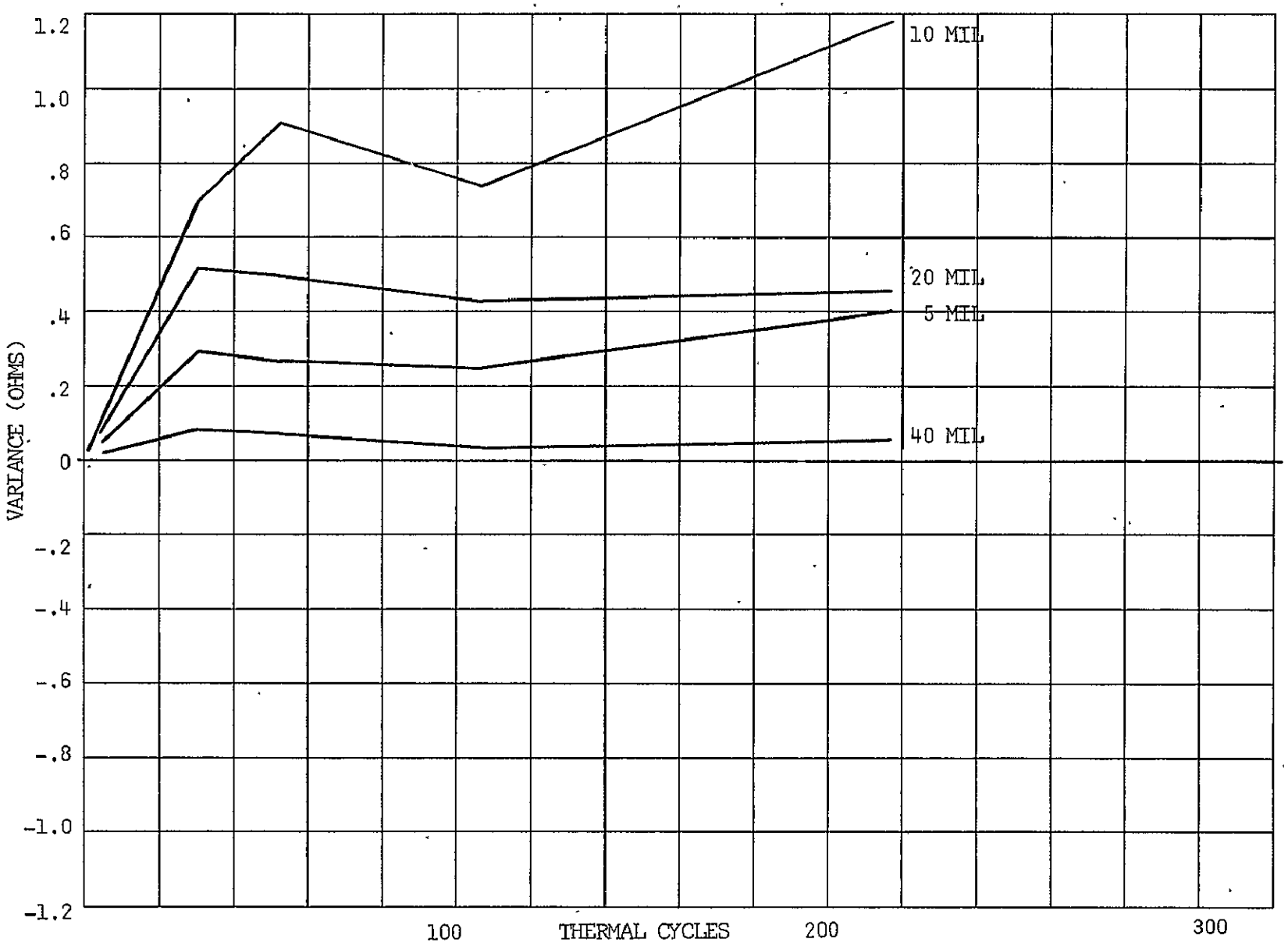


Figure 25. Temperature Effects vs. Line Width (Aluminum Substrate)

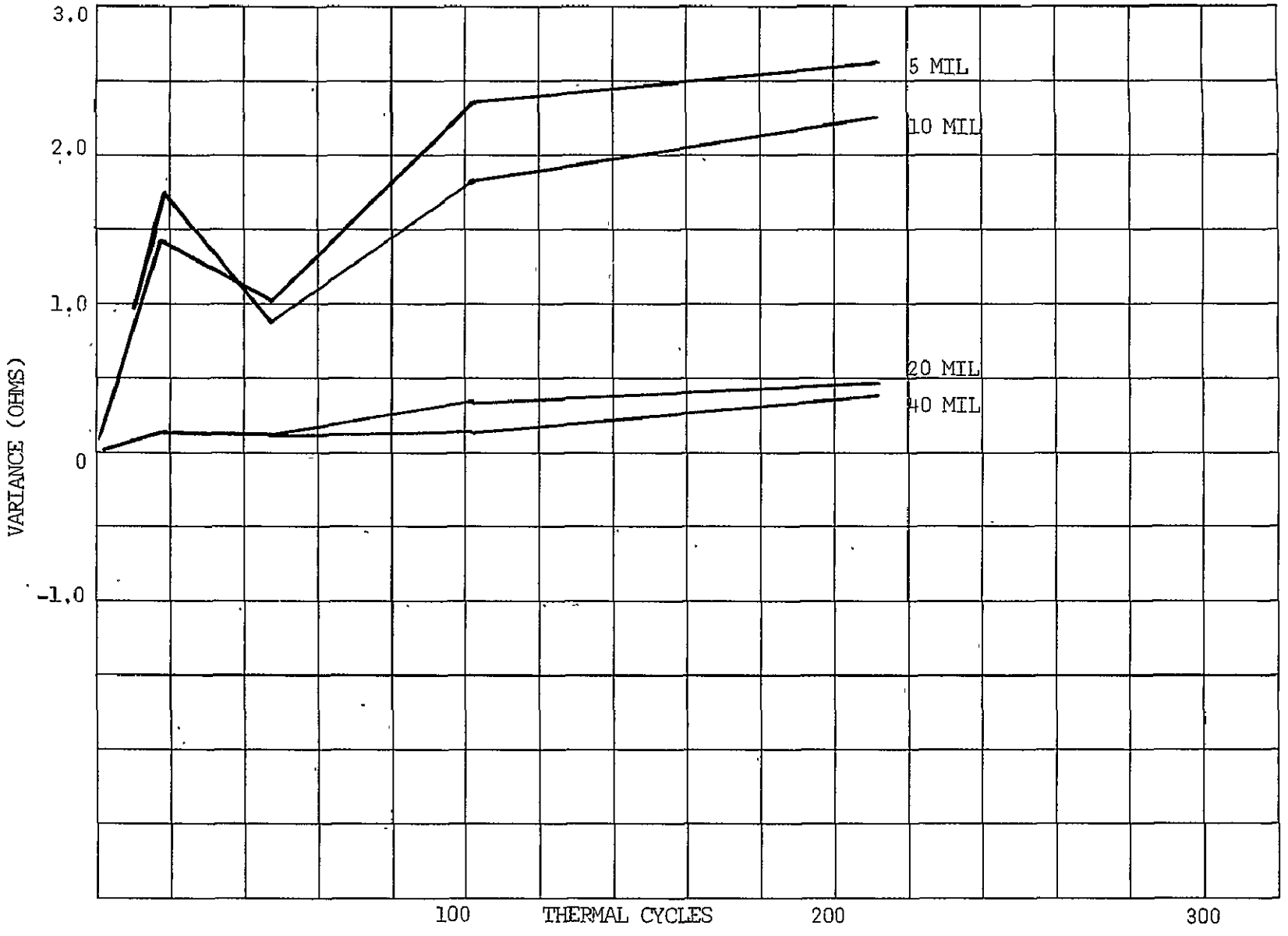


Figure 26. Humidity Effects vs. Line Width (Aluminum Substrate)

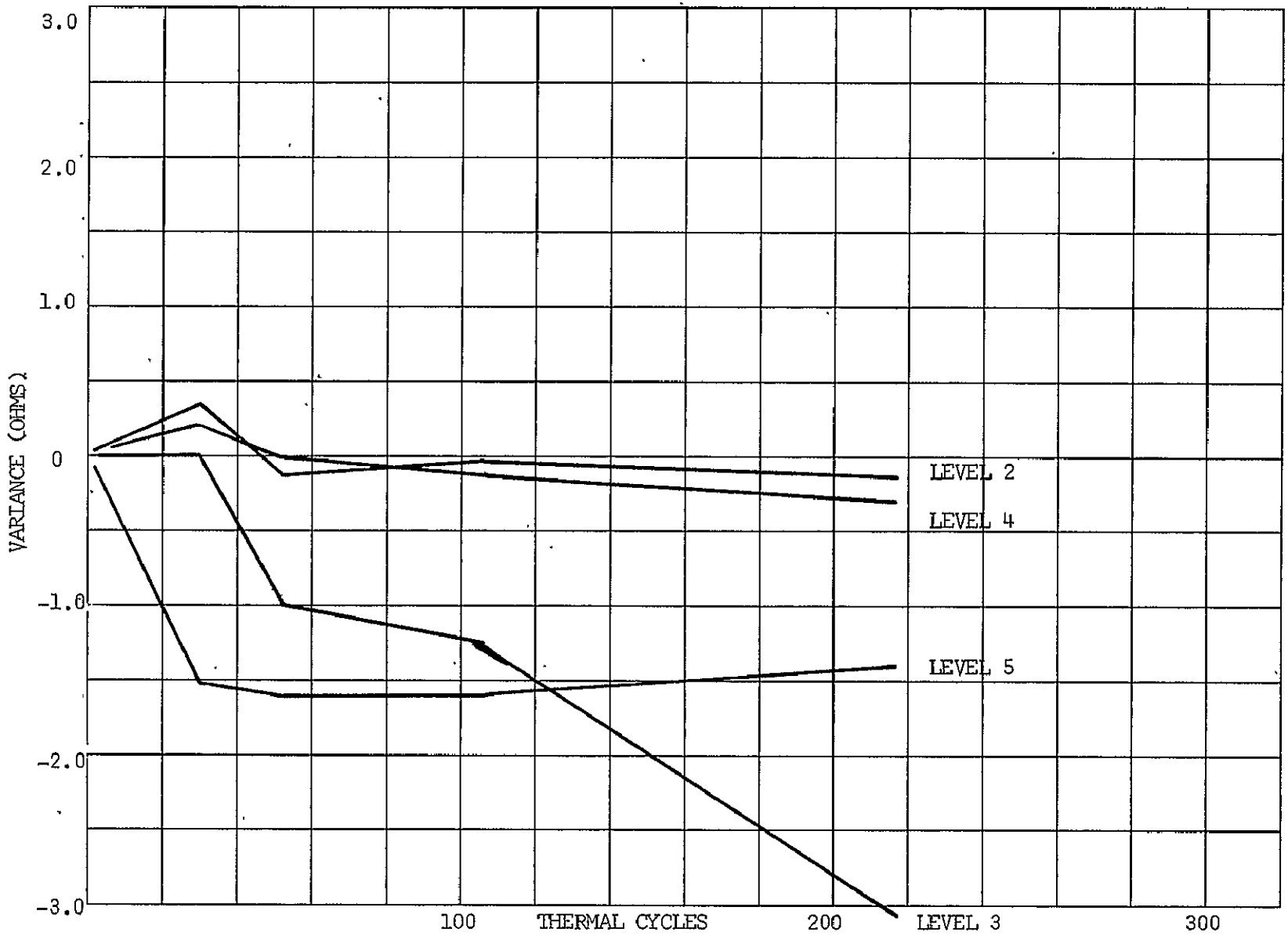


Figure 27. Temperature Effects vs. Layer Depth (Vespel Substrate)

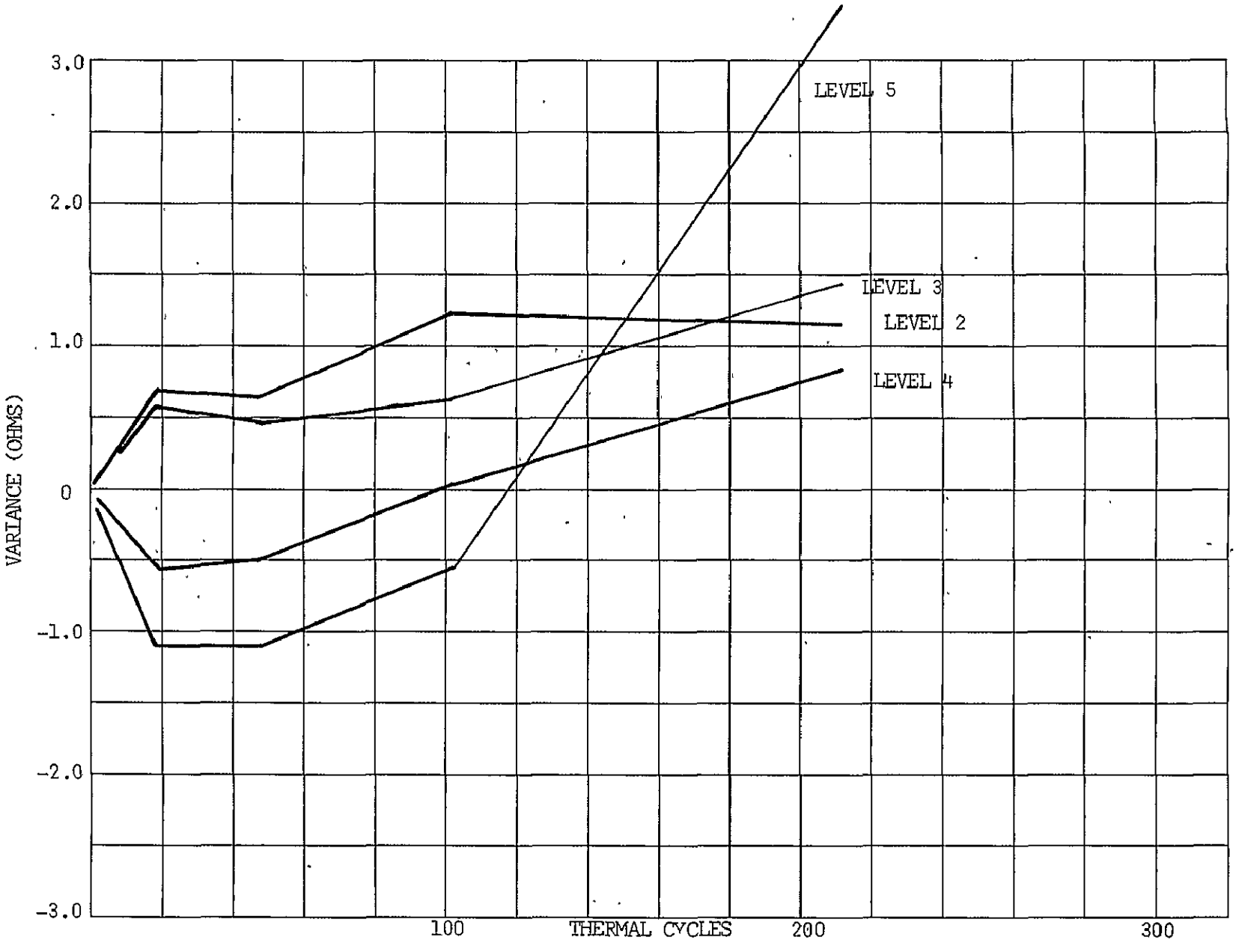


Figure 28. Humidity Effects vs. Layer Depth (Vespel Substrate)

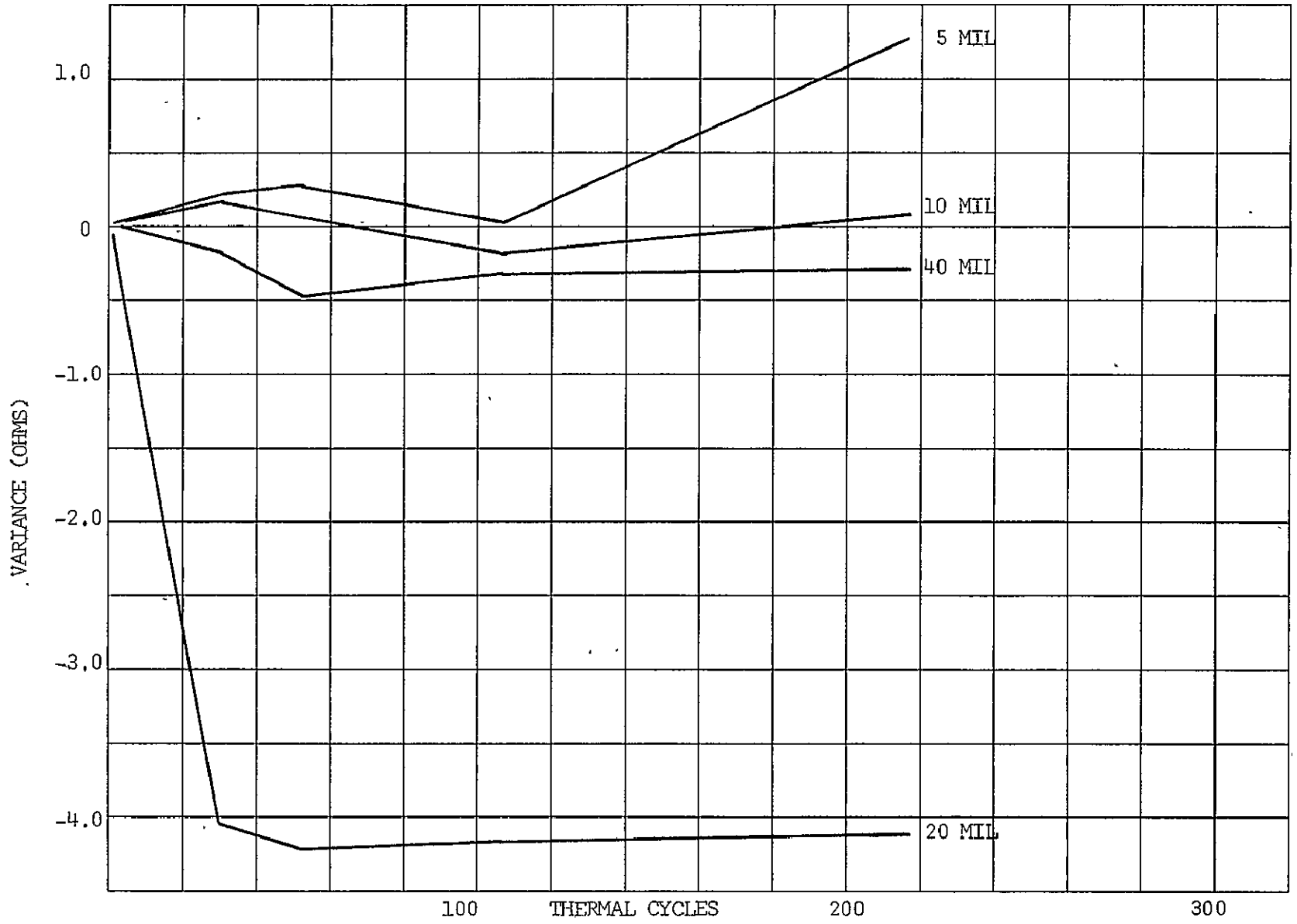


Figure 29. Temperature Effects vs Line Width (Vespel Substrate)

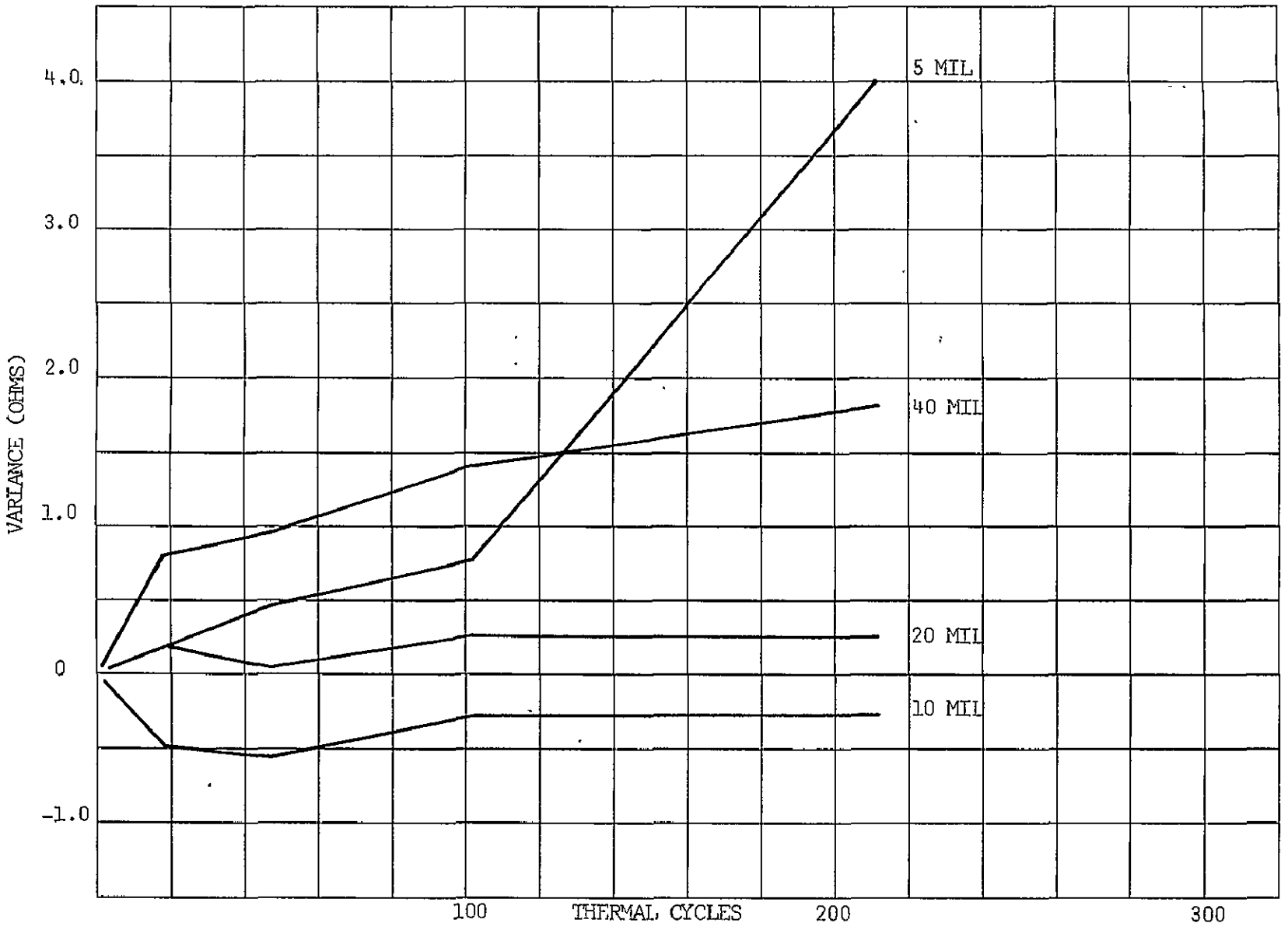


Figure 30. Humidity Effects vs. Line Width (Vespel Substrate)

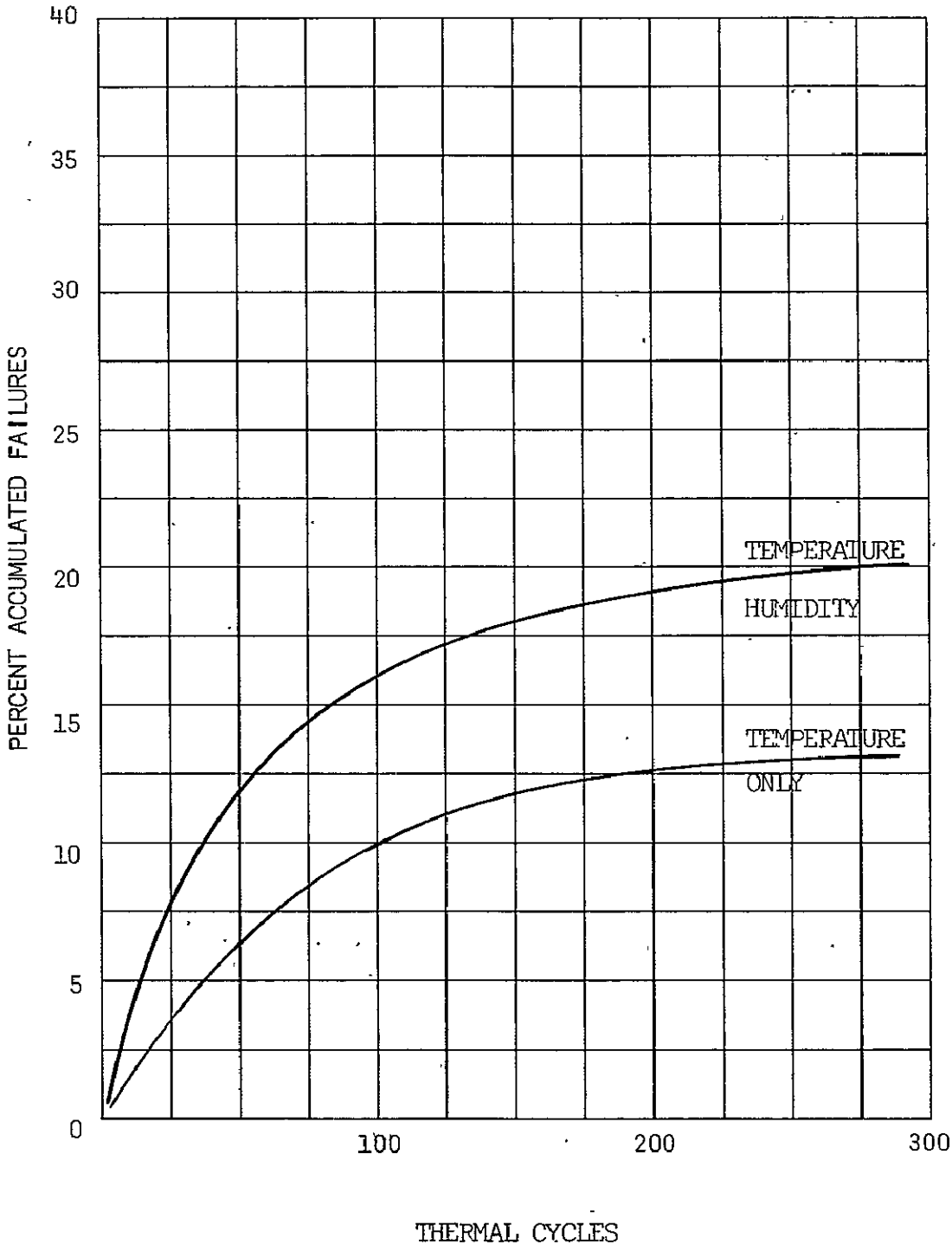


Figure 31. Multilayer Printed Circuit Board Failure Rates

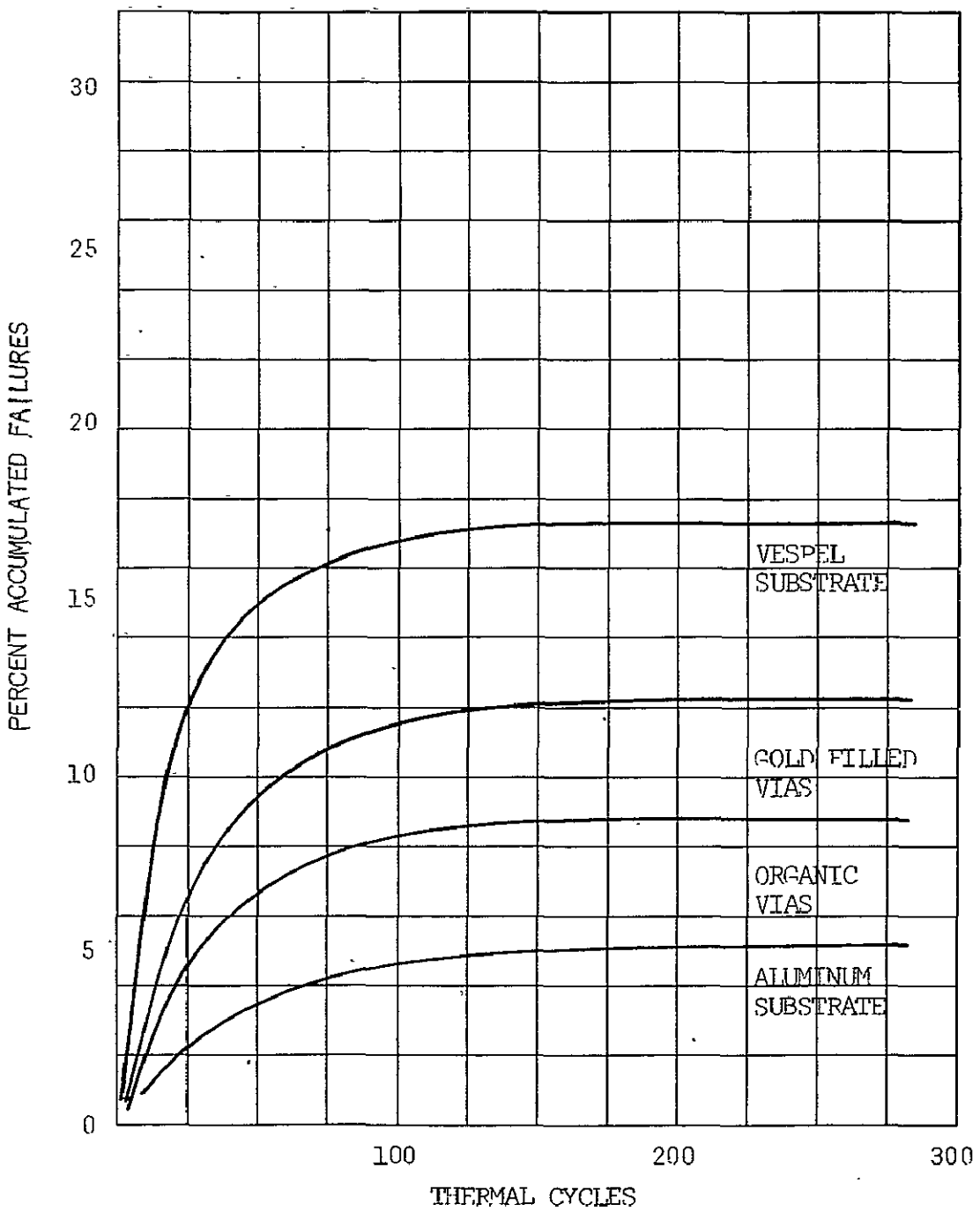


Figure 32. Failure Rate vs Thermal Cycling: Substrate and Via Material

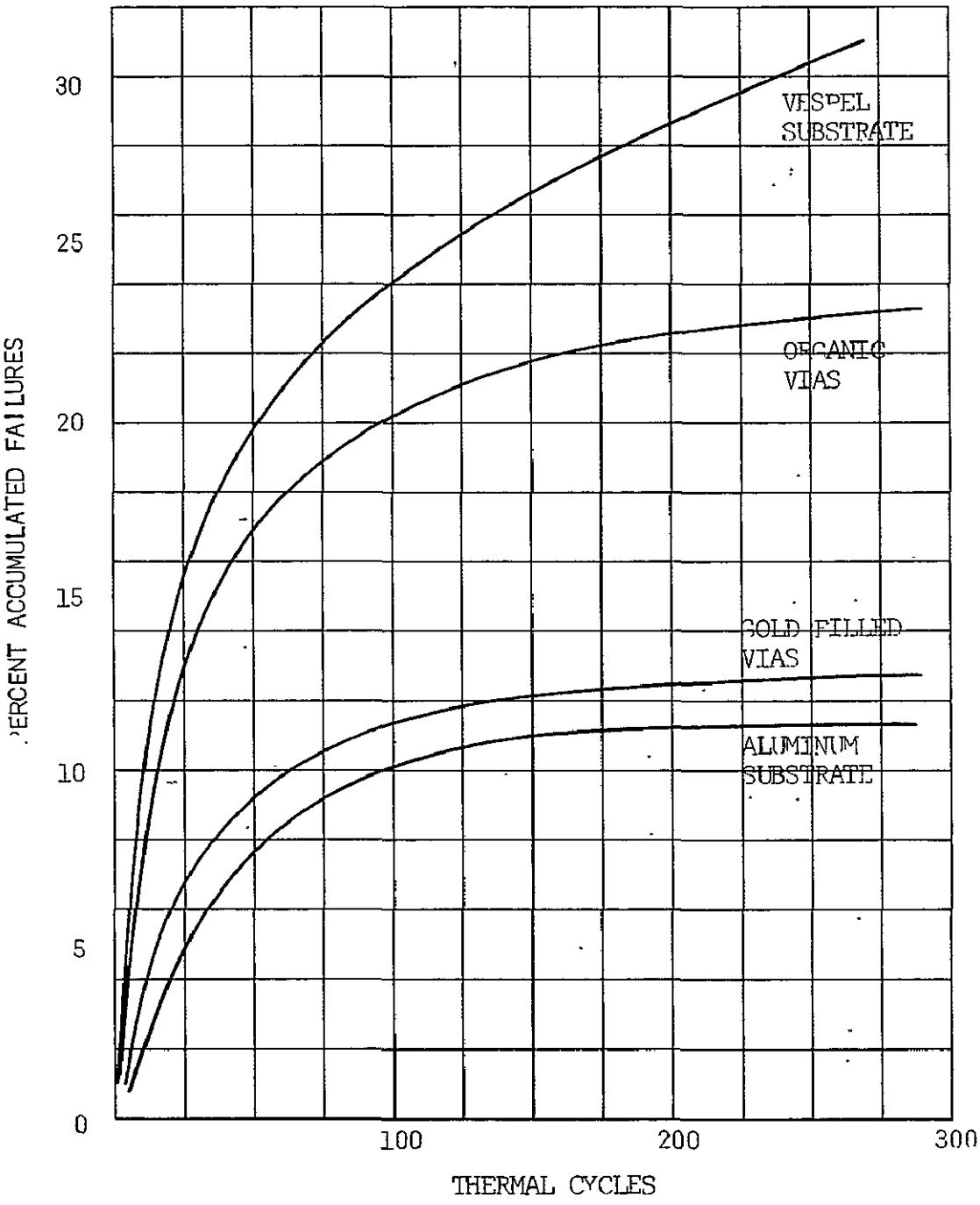


Figure 33. Failure Rate vs Humidity: Substrate and Via Material

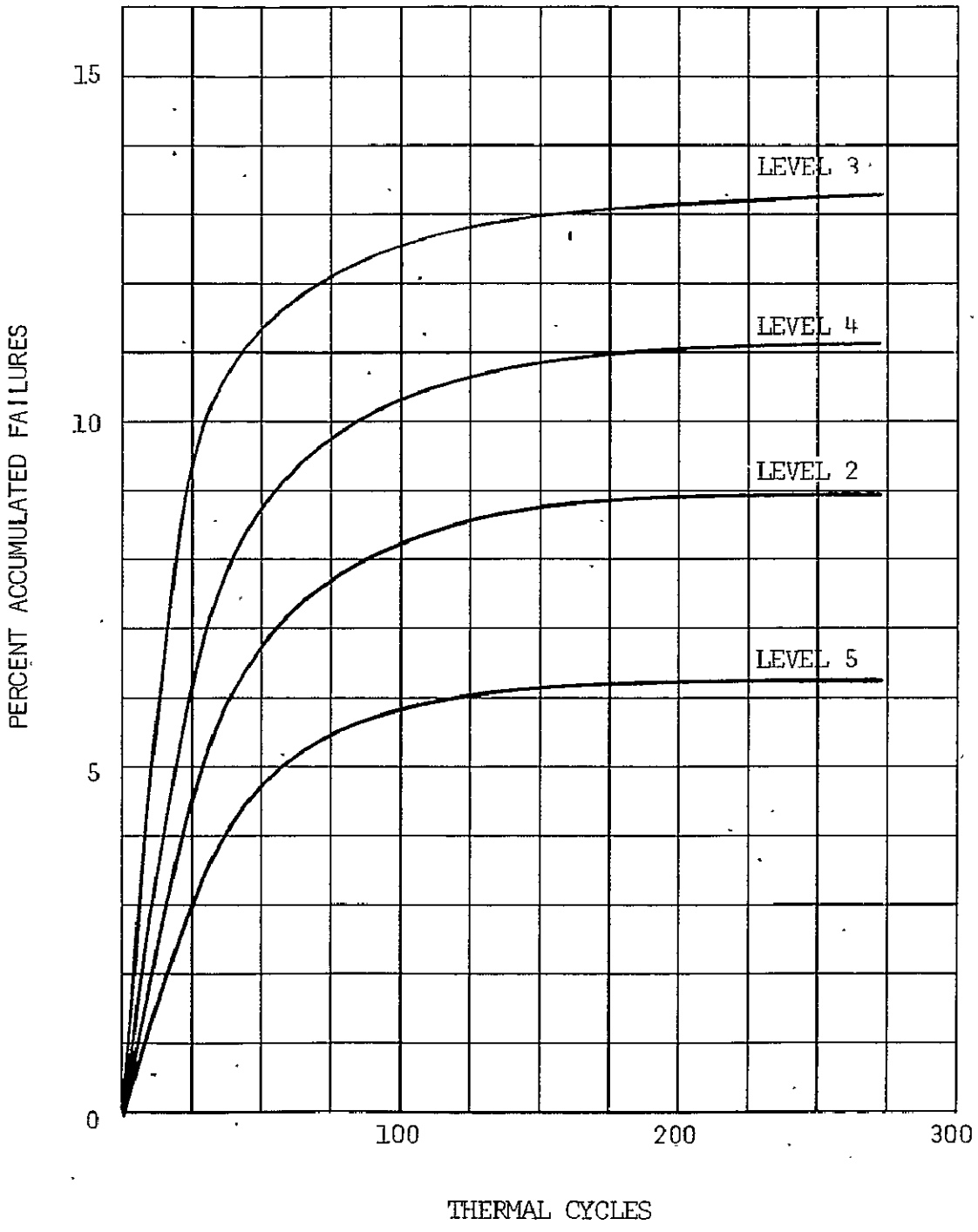


Figure 34. Failure Rate vs Thermal Cycling: Layer Depth

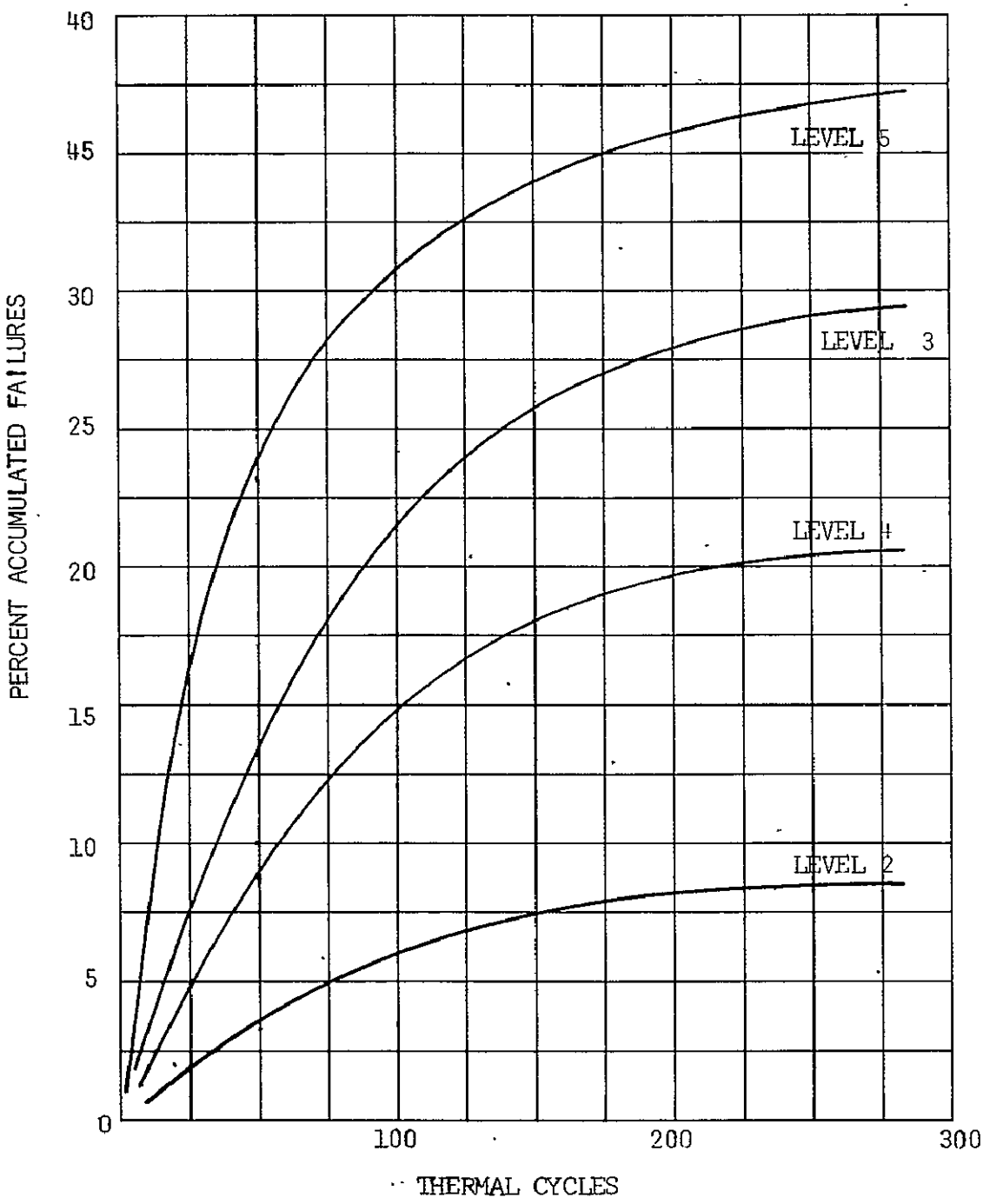


Figure 35. Failure Rate vs Humidity: Layer Depth

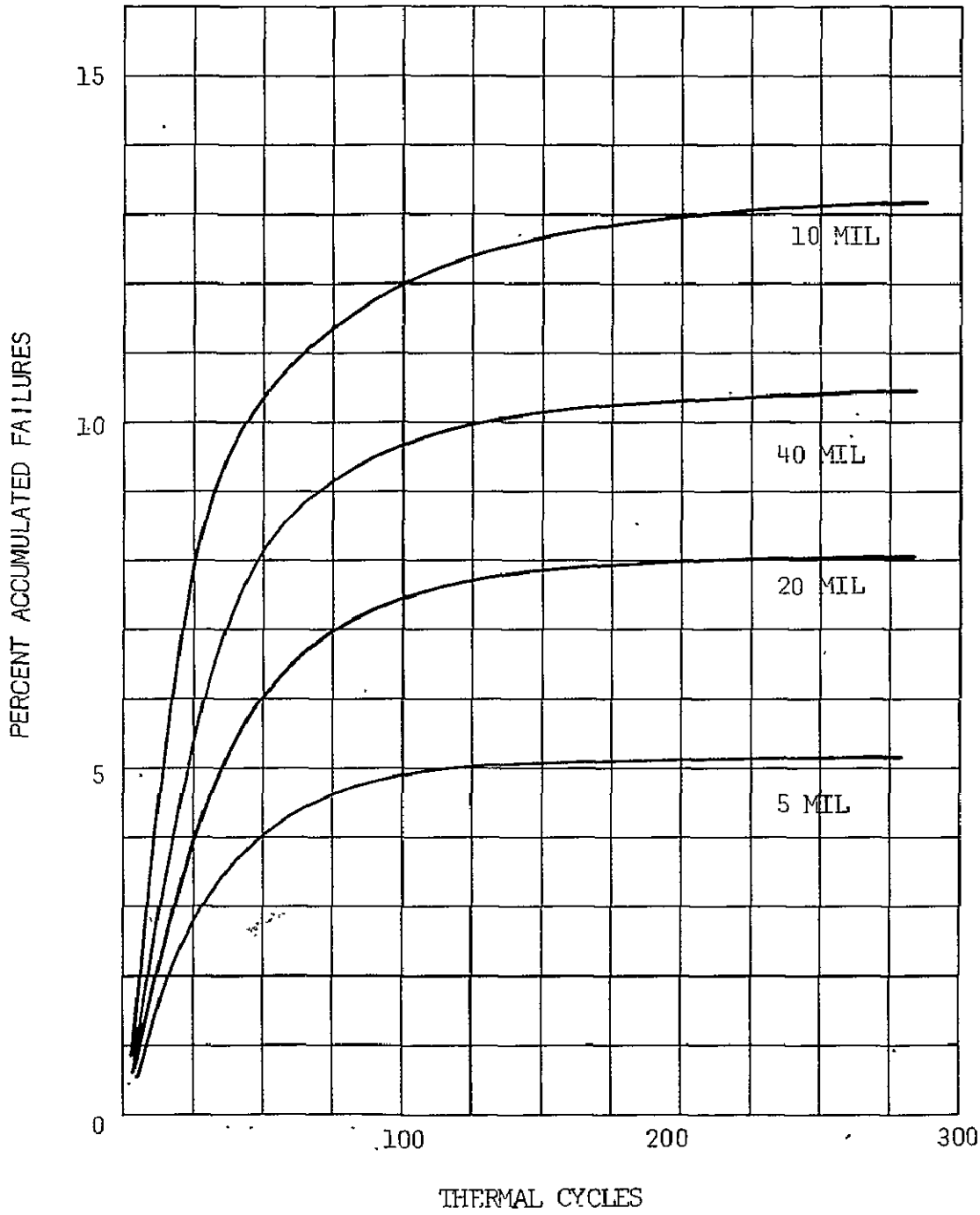


Figure 36. Failure Rate vs Thermal Cycling: Line Width

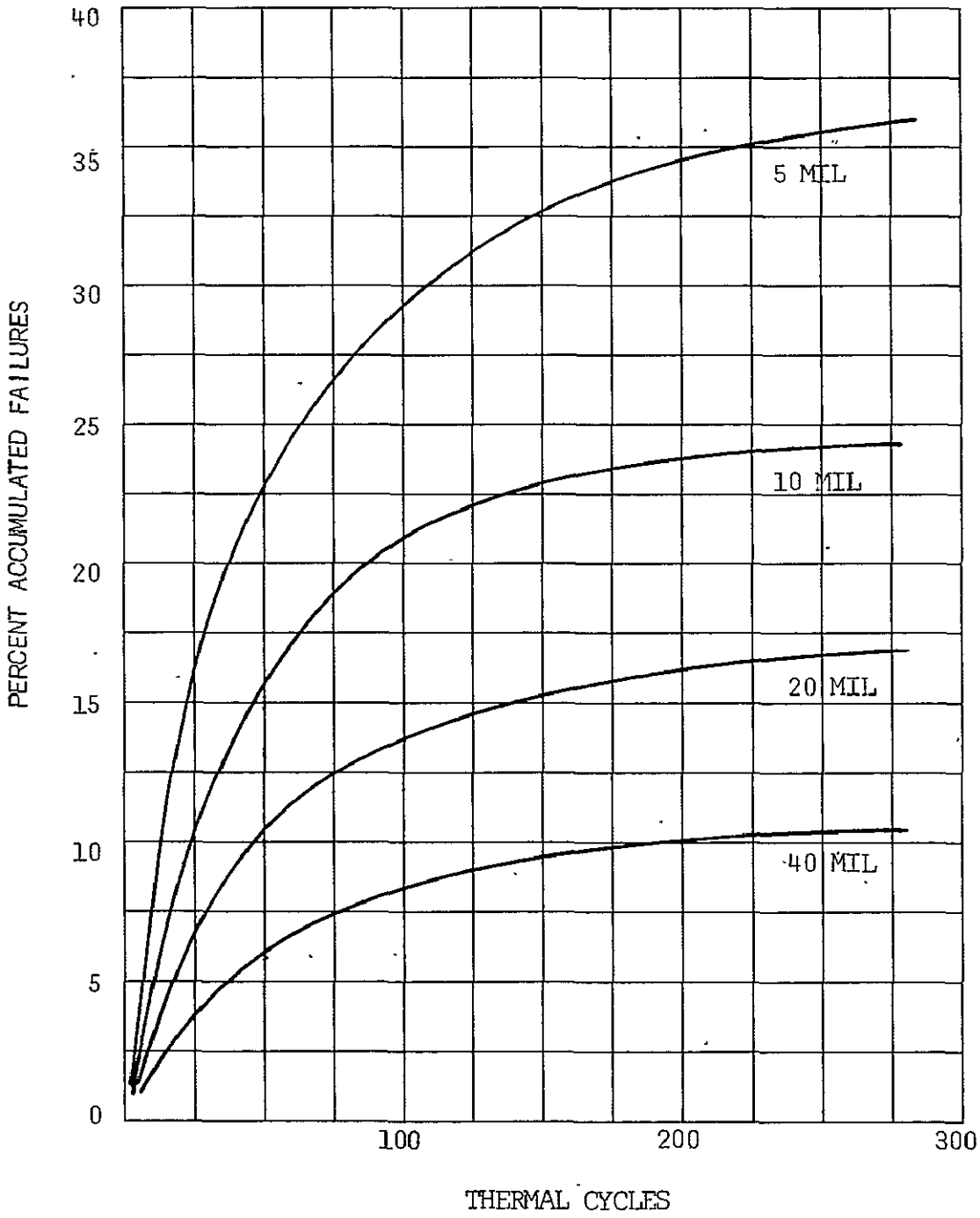


Figure 37. Failure Rate vs Humidity: Line Width

associated with the 40 mil lines. All line widths below this value are associated with increasing resistance values but do not appear to follow a significant pattern. The somewhat surprising stability of the 5 mil lines cannot be accounted for at this time.

Under high humidity conditions, however, the expected trend in decreasing stability with decreasing line width is evident, as shown in Figure 26. This again may be an effect dominated by the mismatch in moisture permeability between the aluminum substrate and the dielectric system.

Turning now to the same analyses for Vespel boards one finds, as shown in Figure 27, a generally negative incremental resistance associated layer depth under thermal cycling. This is in contrast with the corresponding treatment on aluminum substrates (Figure 23). Except for Level 3, these trends appear to be leveling out after 100 cycles. Since the board fabrication is a one-level-at-a-time process, an occasional departure in properties for a given level is not unexpected. No physical explanation is available at present.

The introduction of high humidity also introduces a positive incremental resistance, as shown in Figure 28. Again there appears to be no strong dependence on circuit level. In this case, Level 5 appears to act erratically after 100 cycles while the others seem to be approaching a stabilization. It will be recalled that Level 5 on aluminum substrates (Figure 24) also experienced the highest variance in resistance but that it clearly showed a tendency to stabilize after 100 cycles.

Figure 29 shows the effects of thermal cycling on resistance variance as a function of line width, again on Vespel substrates. As with the aluminum substrates (Figure 25) no uniform trend with respect to line width is apparent and a substantial leveling off is seen to begin after 100 cycles for all except the 5-mil line width. The continuing positive slope for the 5-mil line width may indicate a geometrical limit of design for the technology as it now stands. The trends plotted in Figure 29 again support the possibility of using thermal cycling as a conditioning and stabilizing screen for finished boards.

Figure 20 shows the same line width correlation (on Vespel substrates) under the high humidity treatment. Again the 5-mil line tends to suffer a sharp increase in resistive variance after 100 cycles while those of the other line widths tend to stabilize. This further suggests 5-mil geometry as a present resolution limit. The remaining trends, however, appear to follow a reverse order (cf. Figure 26, on aluminum) with respect to line width progression. Again, moisture transfer to and from the dielectric medium may be a dominating factor. Not only the aluminum but the gold metallizations themselves are effective water transport barriers. In the absence of an aluminum substrate (Figure 30) the line widths themselves may become the controlling factor.

Plots of percent accumulated failures as a function of applied stress cycles also were prepared for comparative purposes. Figure 31 gives an over-all comparison between thermal cycling and high-humidity-thermal cycling. The substantially greater effects of humidity are apparent, but failure rates per cycle (slopes of curves) under both sets of conditions are approaching zero at 300 cycles.

Figure 32 plots cumulative failures as functions of substrate materials and z-direction conductor materials. All failure rates tend toward zero after 100 cycles. It also will be seen that the organic-filled are more stable than the gold-filled vias. The organic substrate (Vespel), however, is associated with the highest total failures and the aluminum, with the lowest. In attempting to explain this difference in substrate

material behavior consideration should be given to the fact that thermal cycling "alone" was conducted in ambient humidity (50 to 65 percent relative) and the effects of moisture were not entirely excluded.

The same plots under high humidity conditions are given in Figure 33 where it will be seen that cumulative failures are substantially increased. Now, however, the organic-filled vias clearly are more vulnerable than the gold-filled vias. The moisture impervious (metallic) systems obviously have diminishing failure rates which show a tendency to disappear after 200 cycles. Not so the organics. Figure 33 confirms graphically a preliminary conclusion reached in the preceding section regarding the special vulnerability of the organics under high humidity cycling from -55 to +100 deg C. The dimensional effects caused by the freezing of sorbed water should have a particularly degradative effect on the interfaces between gold metallizations and z-direction conductors.

Figures 34 and 35 show the effects of thermal cycling and of high-humidity-thermal cycling, respectively, on cumulative failures as a function of layer depth. As generally indicated in the previous plots of resistance variances there appears to be little evidence of a progressive trend associated with layer depth under thermal cycling, although some indication of trend is seen at high humidity (cf. Figure 24 and text). Under the high humidity stress the failure percentages are substantially greater and require a greater number of cycles in approaching a level-off point than is the case under more moderate humidity conditions.

In Figures 36 and 37 are summarized the effects of thermal cycling and high-humidity-thermal cycling, respectively, on cumulative failures as a function of line width. Again no trend with respect to line width is apparent under moderately humid conditions. However, under high humidity conditions the expected progression of vulnerability with decreasing line width is clearly evident. An approach to a vanishing failure rate is in doubt only with respect to the 5-mil line width and once again suggests a 5-mil line and spacing limit in the process as practiced.

The foregoing statistical evaluations do not constitute a complete analysis but only a generalized beginning in the correlation of process treatments with subsequent electrical function. Even as they stand these evaluations may yield additional deductions, or pose additional questions, after a more prolonged consideration. Other evaluations of possible process significance also could be made on the present set of data, such as the interaction of layer depth with line width, or of layer depth with z-direction conductor material, in contributing to failure rates. It also may be possible, through further analysis, to arrive at a more formal definition of failure than the one adopted here. Another unanswered question relates to the significance of "recoveries" (i.e., reversion of a failed circuit resistance to a level below the specified failure level) on prolonged cycling. Are they likely to be permanent? What processing (or materials) factors are involved? Another relatively untouched area is that of erratic resistance readings and their significance with respect to z-direction conductor materials, or the interfaces of these materials with the gold metallizations. However, what does seem clear at this point is that one can achieve thermal expansion compatibility among such diverse materials as plastics and metals but still not arrive at a compatibility in terms of moisture absorption and its possible consequences on dimensional stability. It also appears from the analysis that the technology is limited to a 5-mil minimum geometry and, further, that treatment of the boards to 100 thermal cycles (ambient humidity) has a generally beneficial and stabilizing effect on circuit function which may be employed as a process screen.

CONCLUSIONS AND RECOMMENDATIONS

On the basis of the successful fabrication and environmental stress testing of five multilayer printed circuit boards employing polyimide plastic as the dielectric and a limited use of completely organic conductors, it is concluded that the major program objectives have been met. A basic philosophy of this program has been to remove an important origin of board failure by developing a fabrication technology based on the highest attainable compatibility among the materials used. The long-range aim has been to achieve this result by way of an "all organic" board. The present program constitutes a significant step in the direction of this goal.

Organic dielectrics are not new, and one of the best available today is the class of polymers known as "polyimides". Organic conductors, on the other hand, are much more in the nature of laboratory curiosities and, to date, have not had much practical application. Much of the developmental effort on this program has been spent in formulating such a conductor made from pyrolyzed polyacrylonitrile. The fabrication of electrically functional multilayer boards using these materials confirms the evolution of a workable process.

The compatibilities of the materials employed underwent a severe test in the prolonged thermal cycling of the five boards from -55 to +100 deg C. under both ambient and 90 percent relative humidity conditions. These treatments were monitored by electrical resistance tests of a number of circuit segments, comparable from board to board, at specific cycling intervals. A statistical analysis of the data so obtained pointed to a substantial materials compatibility with respect to thermal expansion properties but a significantly lower compatibility under highly humid conditions. Since not all the conductors were non-metallic, and since some of the supporting substrates also were metallic, a water absorption mismatch between metallic and nonmetallic materials existed on all boards tested. Furthermore, since all of the conductive paths monitored included two, or more, polymer/metallization interfaces, the trends taken by the electrical data represented an acceptable index of the mismatches observed. In a real sense, therefore, the program not only provided a solution to the thermal expansion mismatch problem but also revealed the potential hazards of a water absorption mismatch among the materials of fabrication.

A further outgrowth of the statistical evaluation of electrical data was the repeated indication that a leveling-off, or stabilizing, effect was produced in circuit resistance after 100 to 150 thermal cycles. It is expected that a useful screening procedure based on this effect can be utilized in future board fabrication. The analysis also yielded evidence that 5-mil geometry is a resolution limit in the present technology.

It is recommended that further development be carried forward in three general categories: processing improvements, additional environmental stress tests and derivative experiments based on the sum of present experience. In the first category the most important presently existing processing requirement is for a multiple application technique in via filling. This would speed processing and materially reduce costs. It would require tailoring the properties of z-direction conductor formulation for a particular application method (e.g., metal mask, screen, etc.). Another area requiring attention is the present means of protecting exposed gold metallizations from successive

etch procedures. The multiple build-up and cure of polymer films for this purpose is a temporary measure that introduces subsequent difficulties in film removal. This approach could be supplanted by an adequate via-filling technique. A problem of lesser importance (in terms of cost) is the sporadic warping of Vespel substrates. A remedy for this effect should not require a substantial effort. Finally, investigation should be made into means for automating various aspects of fabrication. A minimal step in this direction would be the substitution of mechanical keying for visual artwork alignment. Other steps would be to optimize out of the development stage, and into the production stage, basic process steps, such as cure cycles, which then could be programmed. All such steps taken would effect a reduction in the "operator dependence" referred to in a section of this report.

With respect to additional environmental stress investigations it should be emphasized that the data presented in this report provide a substantial performance base-line on which to make comparisons with other multilayer board specimens. One obvious comparison would be with the failure rates on conventional epoxy-glass boards subjected to the same stress regime. Boards representing new departures in fabrication technology also could be evaluated on a comparative basis. Another existing foundation for further work is the statistical evaluation derived from the stress data of this report. An opportunity exists for deriving additional conclusions from the present analysis, of expanding the analysis to include other correlations and of delving deeper into the physical significance of the correlations. The quick-trend graphical presentation in this report can be regarded as an initial basis for further inquiry into the meaning of the data obtained.

An obviously important objective in further environmental stress tests would be to establish circuit failure rate as a function of absorbed water solidification at freezing temperatures. This objective could be approached in several ways:

1. A board could be electrically wired, and the function of its circuits continuously monitored, over repeated high humidity cycles across the freezing point

2. Strain gauges could be affixed to a board and monitored under a similar regime

3. A board, or set of boards, could be cycled at high humidity without external electrical connection but resistance monitored at fixed intervals (as has been done on the present program) in two consecutive series, the first cycles from +5 to +100 deg C, the second, from -10 to +100 deg C. Failure rates applicable to the two series then could be compared.

Establishment of a significant degradation effect in association with water solidification would help clarify future design and materials considerations.

The ubiquity of atmospheric water demands that moisture penetration be dealt with in one way or another. Some derivative experiments aimed in this direction would be to coat present boards to "equalize" water transport from both sides in order to set up opposing stresses that dimensionally cancel each other. This might be achieved simply by coating the backs of Vespel boards with a varnish thickness

approximating that of the opposite side. Another approach would be to render the board completely impervious by means of a hydrophobic coating – particularly a metallization. Alternative to surface treatments is the "bulk" approach which freely admits penetration of water but requires that the materials of fabrication match each other in water absorption as well as thermal expansion properties. This objective essentially demands continued development in the direction of the "all organic" board.

On the basis of progress made to date in the fabrication of boards from materials of improved compatibility, and of the promising endurance of circuit function demonstrated on such boards under extended environmental stressing, investment in a follow-up program is recommended in which the more important investigations itemized in the above three developmental categories are undertaken.

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